

# TP3410 2B1Q U Interface Device User's Manual

National Semiconductor  
Application Note 913  
Willie Picken  
Chris Stacey  
August 1994



TP3410 2B1Q U Interface Device User's Manual

## OVERALL INDEX

### Part I TP3410 Circuit Details and Applications

This part of the document describes the TP3410 Circuit details as well as the use of the device in a number of applications.

### Part II TP3410 Software Driver Considerations

This part of the document describes software driver considerations for practical applications. This document is updated to cover enhancements in TP3410 Rev 3.3 and Rev 3.4 devices.

## APPLICATIONS CONTACTS

The information in this manual supplements the TP3410 Datasheet in the Telecom Databook 1994. This document is updated to cover enhancements up to Rev 3.4 of the TP3410. NSC ISDN applications departments may be contacted at the following addresses:

National Semiconductor Corporation  
MS D2-707

2900 Semiconductor Drive, Santa Clara, California 95051,  
U.S.A.

Fax: (408) 733-0613

In USA Contact:

- Richard Tuck  
General Applications, & All Documentation  
Phone: (817) 468-6962  
or  
(800) 272-9959
- Willie Picken  
Hardware, Software & Applications  
Email: willie@berlioz.nsc.com,  
Phone: (408) 721-3283  
Fax: (408) 733-0613

In Europe (Germany):

- Bart Vos  
Hardware, Software & Applications  
Email: cbavge@tevm2.nsc.com  
Phone: (49) 81-41-103411  
Fax: (49) 81-41-103 220

In SEA (Hong Kong):

- Raymond Au-Yeung  
Email: ctcahk@tevm2.nsc.com  
Phone: (852) 737-1702  
Fax: (852) 736-9931

AN-913

## Part I. TP3410 Circuit Details and Applications

### INDEX

#### 1.0 EXTERNAL COMPONENTS

- 1.1 Crystal Manufacturers
- 1.2 Master Clock Design Considerations
- 1.3 Line Transformer Vendors
- 1.4 Standard Line Interface Circuit Design Considerations
- 1.5 Alternate Line Interface Circuit Design Considerations

#### 2.0 PROGRAMMING THE TP3410

- 2.1 Enhanced Microwire Port

#### 3.0 ACTIVATION STATE TABLES

- 3.1 Finite State Transition Matrix LT/NT
- 3.2 Device State Flow Diagrams LT/NT

#### 4.0 TYPICAL EXAMPLES OF ACTIVATION/DEACTIVATION

- Normal DSL Start-Up LT/NT Initiated
- DSL Tear-Down Normal Mode/Line-Break
- Extended DSL Start-Up LT/TE Initiated

#### 5.0 TEST ACCESS

- 5.1 Pulse Transmission Test Modes
- 5.2 NT1 Maintenance Modes

#### 6.0 APPLICATIONS DIAGRAMS

- 6.1 8 Channel Line Card
- 6.2 NT-1
- 6.3 Regenerator
- 6.4 POTS Pair-Gain (Digital Add-on Main Line) and LT Master Mode

#### 1.0 EXTERNAL COMPONENTS

##### 1.1 Crystal Manufacturers

Specifications for the crystal are: nominal frequency of 15.360 MHz parallel mode, frequency tolerance less than  $\pm 60$  ppm, with  $R_s < 20\Omega$ ,  $C_L = 20$  pF, CO (shunt capacitance)  $< 7$  pF. Some U.S. vendors of suitable crystals include:

- Monitor Products Co. Inc.  
P.O. Box 1966,  
Via Del Monte,  
Oceanside, CA. 92054.  
Phone: 619-433-4510  
Part Number MM49N1C3A-15.360 MHz
- NEL Frequency Controls, Inc.  
357 Beloit Street,  
Burlington, WI. 53105.  
George Trower  
Phone: 414-763-3591 x312  
Fax: 414-763-2881
- Nymph,  
151 Laura Lane,  
Palo Alto, CA. 94303.  
Phone: 415-856-6900.  
800-227-8974.  
Fax: 415-856-4732  
Part Number NE18A

- CAL Crystal Lab Inc/Comclock Inc.,  
1142 North Gilbert Street,  
Anaheim, CA. 92801.  
Phone: 714-991-1580.  
800-333-9825.  
Fax: 714-491-9825  
Part Number CCL-6-15.360J14F

#### 1.2 Master Clock Design Considerations

The Master Clock source may be either an external signal source at 15.36 MHz or an on-chip oscillator using an external 15.36 MHz quartz crystal. These options are available in both NT and LT modes of the device. Both NT and LT receivers are designed to operate with  $> \pm 150$  ppm tolerance.

To meet ANSI T1.601 test conditions for sending a free running 10 KHz  $\pm 5$  ppm TL or  $\pm 100$  ppm TN tone it may be necessary to have a more tightly toleranced Master clock. The 10 KHz detectors in TP3410 receiver can easily detect 10 KHz with over 150 ppm tolerance.

#### CRYSTAL OSCILLATOR

The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of  $< \pm 100$  ppm total, both to meet the ANSI specification and to allow sufficient lock-in range for the DPLL's to lock to backplane clocks with up to  $\pm 50$  ppm deviation from nominal frequency. This specification must span the conditions of full operating temperature range (commercial or industrial) and effects due to aging and part-to-part parameter variations.

To use the on-chip oscillator circuit and meet this total tolerance with modest costs for the crystal, it is reasonable to buy the crystal toleranced to  $< \pm 60$  ppm, then design the complete oscillator circuit to meet  $\pm 80$  ppm with components variations, and allow a further  $\pm 20$  ppm for temperature and aging.

The crystal is connected between pin 21 (MCLK/XTAL) and pin 20 (XTAL2), and requires a total of 40 pF capacitance from each pin to ground, to provide the 20 pF total load capacitance ( $C_L = 40$  pF in series with 40 pF) used when the crystal is trimmed in manufacture. Typically this should consist of a 33 pF capacitor from each pin to ground as shown in the datasheet, but this value must include any trace and lead capacitance on the board. Each XTAL input pin provides an additional load of about 7 pF. Mica or high-Q ceramic capacitors should be used; NP0 (Negative-Positive Zero coefficient) ceramic capacitors are highly recommended to ensure tight tolerance over the operating temperature range.

An external circuit may also be driven directly from the pin XTAL2 (pin 20) provided that the load presented is greater than 50 k $\Omega$  shunting the 33 pF capacitor. The voltage swing is typically 1V to 4V, so a single CMOS gate input is suitable, but not TTL. Note, however, that the crystal oscillator is inhibited when the TP3410 is powered down, so this method is not suitable for running the Microcontroller which initializes the TP3410, since it could then never be powered up!

#### EXTERNAL OSCILLATOR

As an alternative, an external 5V drive clock source may be connected to the MCLK (pin 21) input pin of the TP3410. In this arrangement, the XTAL2 (pin 20) must be left open-circuit. The nominal frequency should be 15.36 MHz with a tolerance of  $\leq \pm 80$  ppm to allow for temperature and aging (consult manufacturer's data). This oscillator may be shared between a number of TP3410s if required (such as on a multi-channel line card), and may free-run relative to the

backplane clocks (FS and BCLK) when using the Digital Interface in slave mode. No external PLL is required, as the TP3410 includes a DPPLL to lock to and de-jitterize the FSA input from the backplane, and elastic data buffers to absorb clock "wander" between the line side and the Digital Interface with no "slips".

Crystal oscillator board layout is critical to minimize radio-frequency interference. Use short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins), and keep them far from the line interface circuit. On multi-layered boards a ground-plane layer is advantageous to prevent coupling between signals on adjacent board layers. Ground traces on either side of the high frequency trace also help to isolate the noise pickup.

### 1.3 Line Transformer Vendors

Following is a list of vendors of 1:1.5 transformers which have been designed for use with the TP3410 UID. Extensive evaluation has now been done by National Semiconductor on samples from each vendor to verify that the pulse mask and impedance requirements are suitable and that the transmission performance is as good as possible. National Semiconductor has not assessed the longitudinal balance performance, the line fault protection requirements or the manufacturing tolerances to meet any of the specifications in production. Users should confirm these and similar parameters directly with the vendor.

In the U.S. the transformer vendors are:

- Schott Corp. (Nashville).  
Phone 615-889-8800,  
ask for John Marshall.  
Part Number 13781.  
Part Number 14147.

- Midcom (SD).  
Phone 800-643-2661,  
ask for Don Rigdon.  
Part Number 671-6988.
- Pulse Engineering (San Diego).  
Phone 619-674-8100,  
ask for Telecom Products  
Part Number PE 65583.  
Part Number PE 65584.
- Valor Electronics, Inc.  
Phone 619-537-2619,  
ask for Carrie Munson  
Part Number PT 5065.

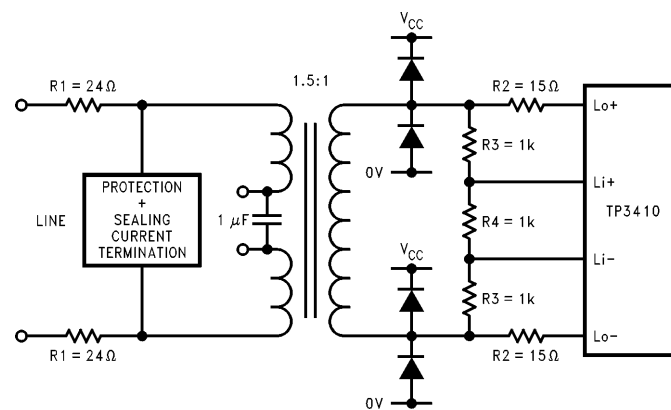
### BER Performance Results of TP3410 Rev 3.2/3.3

BER versus noise margin performance of Rev 3.2/3.3/3.4 devices is equal to or slightly better than Rev 3.1 devices over all loops. The performance of Rev 3.2, 3.3 and 3.4 parts is significantly better than Rev 2.8 devices over all mandatory ANSI and ETSI loops. In particular, loop 4 margin performance surpasses the specified NEXT value of +6 db for both LT and NT. The occasional error condition (for Rev 2.8s) on loops 7 and 15 has been resolved and hence noise margin for all ANSI mandatory loops (4-15) exceeds specification. Rev 3.2, 3.3 and 3.4 devices work reliably over ANSI Optional Loops 1-3.

**Please contact Telecom/WAN applications for the latest information.**

### 1.4 Standard Line Interface Circuit Considerations

In the TP3410 datasheet, *Figure 9* shows the standard line interface circuit, and the text stresses the importance of adhering to this circuit.



**Note 1:** Resistors should be 1% tolerance, except R1 (0.1%) if low impedance to ground at center tap.

**Note 2:** See Table I for optimized resistor values.

**FIGURE 1. Typical Standard Line Interface Circuit, with Nominal Resistor Values**

TL/H/11933-1

The Pulse mask amplitude is set by R1, R2 and the transformer loss parameters. R2 is also constrained as part of the adaptive hybrid circuit of the TP3410. The differing designs from various vendors have different loss parameters leading to different optimum resistor values. Table I shows these optimum resistor values.

**TABLE I. Resistors for Different Transformers for Optimum Performance (Standard Line Interface Circuit)**

Transformer	R1 Ohms (1%)	R2 Ohms (1%)
Schott 13781	24	16.5
Schott 14147	20	16.5
Pulse PE65583/4	24	16.9
Midcom 671-6988	24	17.4
Valor PT-5065	24	16.2

A number of system parameters are affected by the design of the interface circuit, and the inevitable trade offs have been carefully toleranced and tailored to match the design of the TP3410. Nevertheless, there are some ways in which the circuit can be modified, but they required a more complete understanding of the effects on the transmission performance of the system. First, here are some of the more critical parameters which were taken into accounts in the design.

- The local echo path loss ( $Lo \pm$  to  $Li \pm$ ) should be maximized to simplify the task of the echo canceller. 12 dB of external echo path loss is provided by the circuit.
- The transmit path insertion loss ( $Lo \pm$  to line) should be minimized in order to meet the transmit pulse mask and power specifications without excessive power consumption on the chip. The circuit has 3.1 dB of transmit pulse insertion loss, and the TP3410 output amplitude is trimmed to meet the  $\pm 2.5V$  amplitude specification in the pulse mask test with this insertion loss.
- Distortion of the transmit pulses due to transformer saturation should be minimized since non-linear distortion cannot be adequately canceled by a linear echo canceller. The necessary performance has been achieved by the transformer vendors listed above. Further information on transformer distortion specifications can be obtained from NSC Telecom/WAN Applications.
- The input signal swing at  $Li \pm$  must be controlled to avoid overload distortion in the receiver, particularly on very short loops, where the combined signal swing from the two transceivers may reach 15V pk-pk on the line occasionally. Hence the attenuator consisting of three 1 k $\Omega$  resistors is included in the receive path. After the first stage of echo cancellation (the Hybrid Balance Filter) an AGC circuit restores the maximum usable receive signal amplitude, consistent with not overloading the A/D converter.
- Line protection circuit elements may need to be included for surge current limiting, while still meeting the longitudinal balance specification. Hence the 24 $\Omega$  resistors with 0.1% matching are provided, although smaller values may be used, as explained later. This tolerance can be relaxed if the center tap is floating relative to ground.

f. D.C. separation may be required in the center tap of the line side of the transformer to allow the option of line power feeding (hence the 1  $\mu F$  capacitor). The 1  $\mu F$  capacitor value is (as specified in ANSI T1.601) also for identification of the network termination (NT).

g. Taking all the above items into account, the Return Loss specification against 135 $\Omega$  must be met ( $> 20$  dB for  $10 \text{ kHz} < f < 25 \text{ kHz}$ ). The combination of the 15 $\Omega$  termination resistors, the 27 mH transformer with 1:1.5 turns ratio, and the 24 $\Omega$  surge limiting resistors dominate the input return loss. In addition, two stray capacitance elements were factored into the input impedance calculations to allow for the influence of protection devices. Across the primary (device) side, 300 pF was allowed, and across the secondary (line) side 1000 pF was allowed. Other values may be perfectly suitable, but should be taken into account when optimizing the input loss. Values in this range do not impair the transmission performance.

h. The 1  $\mu F$  and other capacitors must have LOW distortion. Use 100V Mylar or Polypropylene types. Do not use electrolytics and be very cautious if considering ceramics.

#### 1.4.1 Surge Current Limiting Resistors

One degree of freedom which is available with the line interface circuit is to modify the value of the surge current limiting resistors, shown as "R1" in Figure 1. 24 $\Omega$  per leg was chosen as the maximum value we have seen used for this purpose on analog lines, and in order to allow the use of tried and trusted protection circuits, this value was designed into the TP3410 interface. There are side effects however. Firstly, these resistors contribute to the common mode input impedance and must be matched to meet the 55 dB longitudinal balance specification. This also depends on the transformer balance, but matching up to 0.1% may be necessary in applications with a low impedance to ground at the transformer center tap (e.g. battery feeding or sealing current sourcing at the LT). This tolerance can be relaxed if the center tap is floating relative to ground.

A second effect of these resistors is to attenuate the received signal thereby degrading the signal-to-echo ratio at the  $Li \pm$  pins.

A third effect is to buffer the line and so reduce the variability of the echo over a range of loops (e.g. as defined in ANSI T1.601). This allows the adaptive hybrid in the TP3410 to operate more efficiently and largely compensates for the degraded signal-to-echo ratio caused by the increased signal attenuation.

#### 1.4.2 Transformer Winding Resistances

Another factor to be taken into account when fixing the resistor values is the winding resistance of the transformer. If the primary (chip side) winding resistance is more than a few ohms then operation of the TP3410 adaptive hybrid will be degraded. The secondary (line side) winding resistance is less critical with effects mostly similar to those of R1 and so can be absorbed into (2)(R1) for design purposes. If the secondary resistance is large, take care over tolerancing to ensure that the pulse amplitude specification can be maintained.

#### 1.4.3 Input Capacitors

With the Revision 2.x or Rev 3.x devices no capacitors should be used on the  $Li \pm$  and  $Lo \pm$  pins.

#### 1.4.4 Protection Devices

Two stages of protection are necessary to ensure the TP3410 is not damaged by over voltage stress. On the line side, a protector such as an **MOV, Transzorb or Sidactor should be used in shunt across transformer**. Although the clamping voltage needs to be low enough to protect the TP3410, it is imperative that this component should not cause clipping of the transmit waveform, which would appear as non-linear distortion on the local echo signal. Since the signal swing on a short loop may reach 15V pk-pk occasionally, a suitable test would be to ensure the protection device impedance exceeds 150 k $\Omega$  measured at 15V pk-pk for 1 kHz < f < 40 kHz.

Alternatively or additionally, **Line Fuse Resistors (LFRs) or PTC** (Positive Temp coefficient) resistors of 9 $\Omega$  typical value may also be added in series with each leg of the line outputs. The value of R1 has to be reduced to 15 $\Omega$  to maintain the effective impedance.

A second level of protection is required on the device side of the transformer to ensure that the voltages on the device pins never exceed the supply, and the figure shows 4 diodes for this purpose. IN4004 or similar are suitable.

#### 1.4.5 Input Impedance and Return Loss Measurement

To measure the input impedance and return loss of the line interface port, it is necessary to ensure that the two R2 terminating resistors provide the correct termination. This can be done either by removing the TP3410, and shorting together the floating ends of the R2 resistors, or by keeping

the chip in the socket and powered up. If the chip is powered up in the socket, it also necessary to disable the 10 kHz Line-signal Detector circuit to prevent interrupts, by means of the following commands:

- X'4400 (PUP);
- X'1A20;
- X'1EC8;

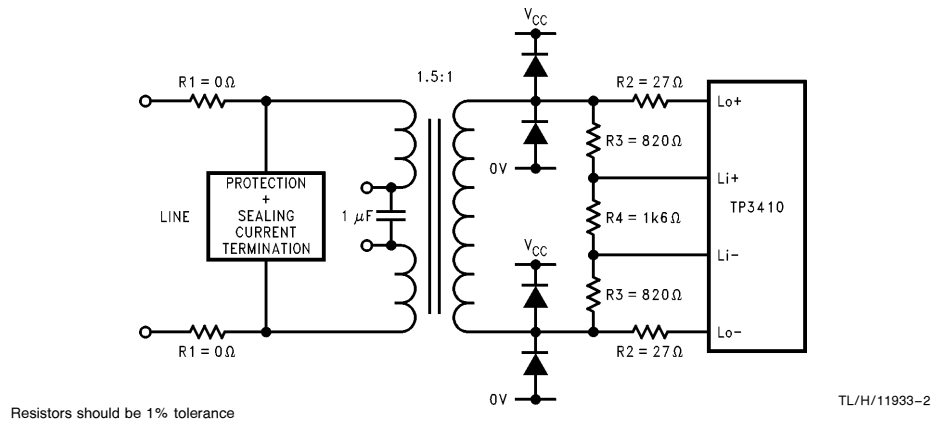
After the measurements, reset the chip before attempting start-up.

Do not make these measurements with the chip powered down since the output amplifier will no longer provide a low impedance between Lo+ and Lo- to correctly terminate the R2 resistors. In Rev 2.x and earlier versions there will be a high output impedance. For Rev 3.x devices a low impedance is provided but measurement will still over estimate the operational (powered up) input impedance.

#### 1.5 Alternate Line Interface Circuit Considerations

An alternative line interface circuit (LIC) configuration is added to the Rev 3.x version of TP3410. This alternative LIC may be preferred in certain line card applications in which power feeding of remote equipment is required. The line side resistors are eliminated and therefore power loss in these resistors is eliminated.

**The standard line interface circuit (Section 1.4) provides better overall performance for very long loops and is therefore recommended wherever possible.**



**FIGURE 2. Alternate Line Interface Circuit, with Nominal Resistor Values**

### 1.5.1 Programming the Device for Alternate Line Interface Configuration

As part of the power-up initialization procedure, program the CR4 register with value X'07, ie. the saif bit (bit 3) is set to 0. For the standard line interface (default condition) bit3 is set to 1.

### 1.5.2 Protection

Protection considerations (see Section 1.4.4) are similar for both LICs. The difference in this case is that the value of a series **PTC** (Positive Temp Coefficient) resistor should be about  $1\Omega$  or less in order to maintain pulse amplitude and return loss specifications.

### 1.5.3 Input Impedance and Return Loss Measurements

The same considerations apply as for the standard LIC described in Section 1.4.5.

## 2.0 PROGRAMMING THE TP3410

TP3410 can be programmed in either microwire mode (MW pin = 1) or GCI mode (MW pin = 0).

Microwire controllers are included in National Semiconductor microcontrollers such as the HPC (16-bit) or the COP (8-bit) family. Motorola microcontrollers with SCP port may also be programmed to work in microwire mode. A TP3464/65 MID Microwire Interface Controller can be used to drive the TP3410 UID from a standard microprocessor such as an Intel 80186 or MC68000.

While in GCI mode, the TP3410 supports the full GCI system control interface. It is necessary to have a GCI controller, such as the TP3451 to communicate the GCI messages to the TP3410.

## 2.1 TP3410 Enhanced Microwire Port

The TP3410 has an enhanced MICROWIRE port such that it can connect to standard MICROWIRE master devices (such as NSC's HPC and COP families) as well as the SCP (serial control port) interface master from the Motorola microcontroller family. SCP is supported on devices such as MC68302 or the MC145488 HDLC.

TP3410 supports two popular formats used in typical terminal equipment applications.

1. CCLK idling LOW when  $\overline{CS}$  pin is inactive HIGH, pulsing LOW/HIGH/LOW for 16 clocks then returning back to LOW for idle condition. Data is output on CO pin on the negative edge and data sampled in on the positive edge of CCLK. This format (shown in *Figure 3a*) is normally used with NSC's microcontrollers from the HPC or the COP8 family.
2. CCLK idling HIGH when  $\overline{CS}$  pin is inactive HIGH, pulsing HIGH/LOW/HIGH for 17 clocks, then returning back to HIGH for idle condition. Data is output on CO pin on the negative edge and data sampled in on the positive edge of CCLK. This format (shown in *Figure 3b*) is normally used with other alternate microcontrollers in the industry, such as the Mot MC68302. The first 16 clock pulses are the normal low-going pulses to shift and sample the microwire data. The **17th pulse needs to be generated with software** by toggling the CCLK clock polarity bit on the microprocessor port. It is necessary to deactivate the  $\overline{CS}$  pin (bring it high) while the CCLK is low as shown in *Figure 3b*.

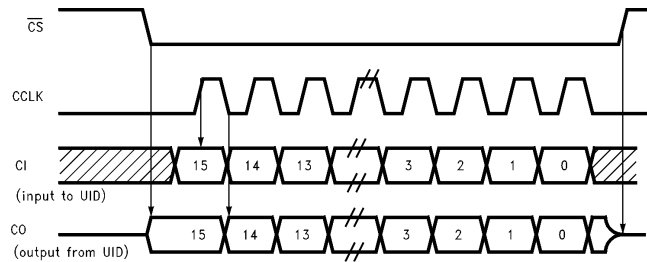


FIGURE 3a. TP3410 Normal MICROWIRE Clock Format

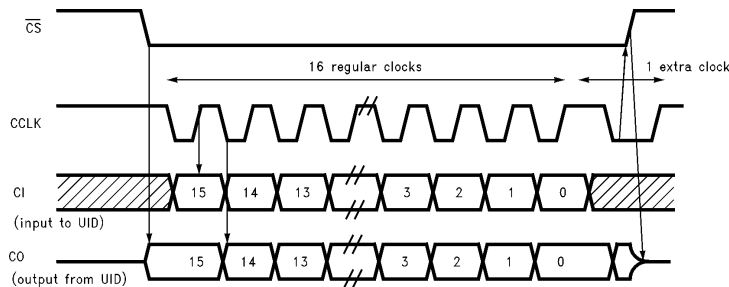


FIGURE 3b. TP3410 Alternate MICROWIRE Clock Format

### 3.0 ACTIVATION STATE TABLES

Two types of activation flow chart are included in this manual. Firstly, the activation state tables from ANSI T1.601 Appendix C are included, with the specific Commands and Interrupts implemented on the TP3410 added.

Secondly, there are flow diagrams showing the state flows and the interactions between the device state machines and the external microcontroller, both in normal and default conditions. Also included are example Interrupt Service routines showing the correct responses to the various interrupts and state changes that occur during the activation sequence.

**The major activation events and signal flow diagrams are shown here. Additional software routines are generally necessary to design a robust practical system. Software device driver considerations are covered in Part II of this Application Note.**

#### 3.1 Loop Start-Up and Tear-Down Finite State Machine Matrix Changes

The following enhancements have been implemented in Rev 3.x devices to comply with the newer ANSI T1-601 spec.:

1. In NT mode, SN2 is delayed until SL2 from the LT is detected (H4 to H6 transition).
2. While in NT mode, the H6 state data transparency is blocked as required by ANSI 601.
3. An LT will not transmit SL1 if there is no NT at the far end. The LT end device will stay quiet and can be reset with the RES command after the expiry of an external 15s timer. If the internal 15s timer is invoked, the device will return to the reset state after the timer expires.
4. The RES command is now effective in PUP or PDN condition. It is also effective in additional states shown in the tables on the following pages.
5. While in H12 or J12 (Receive Reset state), detection of a wake-up tone from the far end will cause a Rev 3.x device to immediately stop the 40 ms timer, generate a DI interrupt and then jump to H1 or J1; in this state it will generate the line-signal detect interrupt (LSD for NT end or AP at the LT end). This enhancement allows the software to reset its flags after the DI interrupt before proceeding with a new activation.

**TP3410 ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN LT MODE (REV 3.x)**

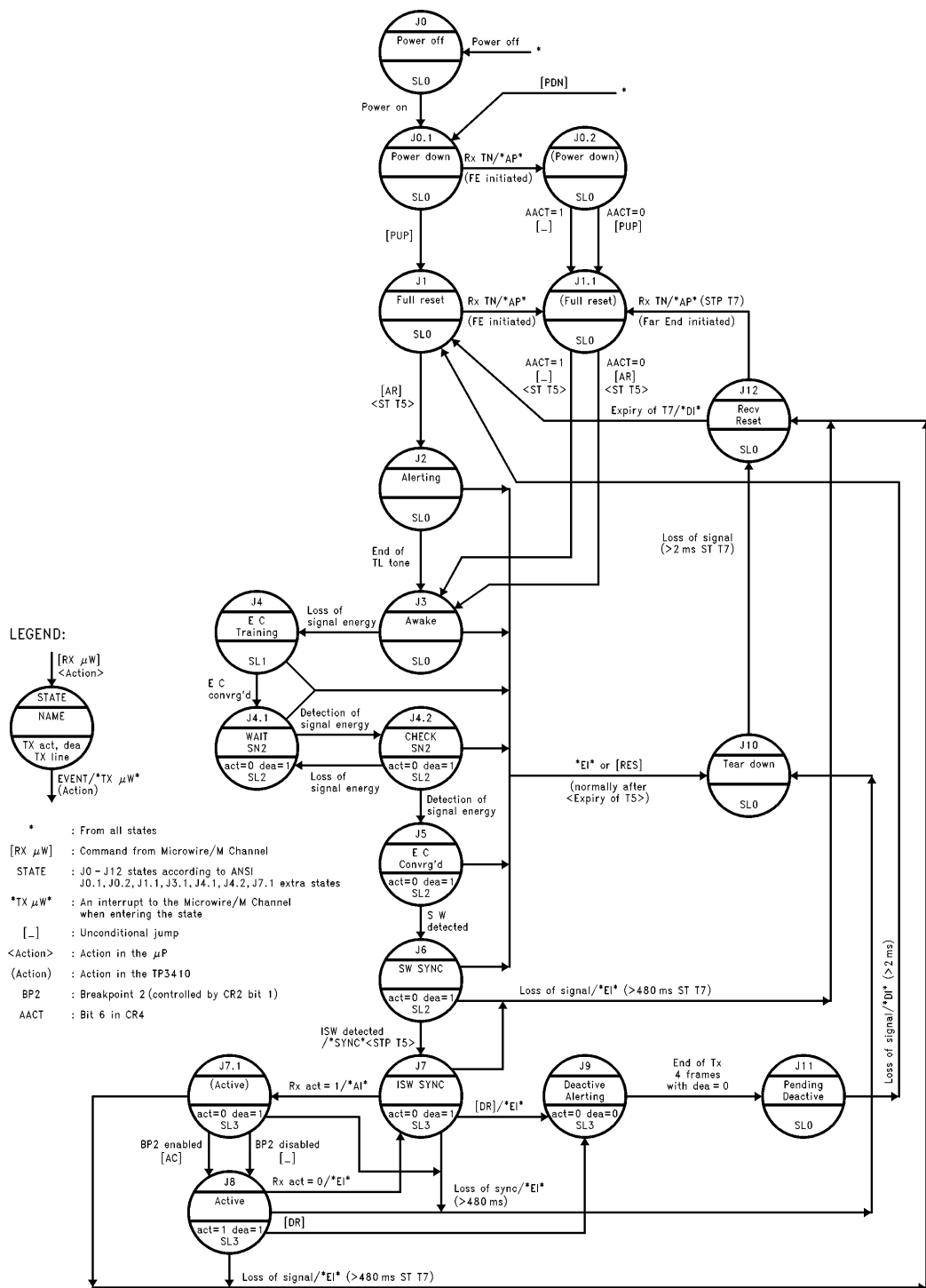
EVENT	STATE NAME	Power Off	Full Reset	Alerting	Awake	EC Training	WAIT SN2	CHECK SN2	EC Covrg'd	SW Sync	ISW Sync	Active	Deact'n Alert'n	Tear Down	Pending Deact'n	Recv Reset
	STATE CODE	J0	J1	J2	J3	J4	J4.1	J4.2	J5	J6	J7	J8	J9	J10	J11	J12
	TX	SL0	SL0	TL	SL0	SL1	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL3 dea = 1 act = 0	SL3 dea = 1 act = 1	SL3 dea = 0 act = 0	SL0	SL0	SL0
POWER ON		J1														
LOSS OF POWER			J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
ACTIVATION REQUEST (AR)			ST T5 J2													
DEACTIVATION REQUEST (DR)											<b>J9</b>	J9				
END OF TONE TL (3 ms)				J3												
RECEIVED TONE TN and ACTIVATION REQUEST (AR)			ST T5 J3 AP													ST T5 STP T7 <b>DI, J1</b>
LOSS OF SIGNAL ENERGY					J4			J4.1								
ECHO CANCELLER CONVERGED						J4.1										
BASIC FRAME SYNC (SW)									J6							
SUPERFRAME SYNC (ISW)										STP T5 J7 SYNC						
RECEIVED act = 0												J7 EI				
RECEIVED act = 1											J8 AI					
LOSS OF SYNC (> 480 ms)											J10 EI	J10 EI				
LOSS OF SIGNAL (> 480 ms)										ST T7 J12 EI	ST T7 J12 EI	ST T7 J12 EI				
END OF THE LAST SUPERFRAME WITH dea = 0 (4th)													J11			
EXPIRY OF TIMER T6 (15 seconds)				J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI						
LOSS OF SIGNAL (< 40 ms)														ST T7 J12	J1 DI	
EXPIRY OF TIMER T7 (40 ms)																J1 DI
DETECTION OF SIGNAL ENERGY							J4.2	J5								
RESET COMMAND (RES)				J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	<b>J10 EI</b>	<b>J10 EI</b>	<b>J10 EI</b>		<b>J10 EI</b>	

**Note:** Items in **Bold** are changes in Rev 3.x devices.



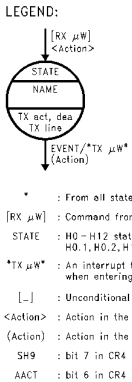
TP3410 ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN NT MODE (REV 3.x)																
EVENT	STATE NAME	Power Off	Full Reset	Alerting	EC Training	WAIT SL	CHECK SL	EC Covrg'd	SW Sync	ISW Sync	Pending Active	Active	Pending Deact'n	Tear Down	TE Inactive	Recv Reset
	STATE CODE	H0	H1	H2	H3	H3.1	H3.2	H4	H5	H6	H7	H8	H9	H10	H11	H12
	TX	SN0 INFO 0	SN0 INFO 0	IN INFO 0	SN1 INFO 0	SN0 INFO 0	SN0 INFO 0	SN0 INFO 0	SN2 INFO 0	SN3 act = 0 INFO 2	SN3 act = 1 INFO 2	SN3 act = 1 INFO 4	SN3 no change	SN0 INFO 0	SN3 act = 0 INFO 2	SN0 INFO 0
POWER ON		H1														
LOSS OF POWER			H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
RECEIVED S/T INFO 1 SIGNAL (Received AR)			ST T4 H2													
RECEIVED S/T INFO 3 SIGNAL (Received AC)										H7					H7	
RECEIVED S/T INFO 0 SIGNAL (Received SEI)											H11	H11				
END OF TONE TN (9 ms)				H3												
RECEIVED TONE TL and ACTIVATION REQUEST (AR)			ST T4 H2 LSD													ST T4 STP T6 <b>DI, H1</b>
ECHO CANCELLER CONVERGED					H3.1											
BASIC FRAME SYNC (SW)								H5								
SUPERFRAME SYNC (ISW)									ST T4 H6 AP							
RECEIVED dea = 0										H9 DP	H9 DP	H9 DP			H9 DP	
RECEIVED act = 0 and dea = 1												H7 EI				
RECEIVED act = 1 and dea = 1											H8 AI					
LOSS OF SYNC (> 480 ms)										H10 EI	H10 EI	H10 EI			H10 EI	
LOSS OF SIGNAL (> 480 ms)						ST T6 H12 EI		ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI			ST T6 H12 EI	
EXPIRY OF TIMER T4 (15 seconds)				H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI							
LOSS OF SIGNAL (< 40 ms)							H3.1						ST T6 H12	ST T6 H12		
EXPIRY OF TIMER T6 (40 ms)																H1 DI
DETECTION OF SIGNAL ENERGY						H3.2	H4									
RESET COMMAND (RES)				H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	<b>H10 EI</b>	<b>H10 EI</b>	<b>H10 EI</b>	<b>H10 EI</b>		<b>H10 EI</b>	
<b>Note:</b> Items in <b>Bold</b> are changes in Rev 3.x devices.																

### State Diagram for the TP3410 in LT Mode



TL/H/11933-5

### State Diagram for the TP3410 in NT Mode



TL/H/11933-6

#### 4.0 TYPICAL EXAMPLES OF ACTIVATION/DEACTIVATION

##### Assumptions:

- TP3410 in the LT has the Breakpoint disabled (BP2 = 0).
- TP3410 in the Regenerator on the upstream side is in NT Mode.

- TP3410 in the Regenerator on the downstream side is in LT Mode with the Breakpoint enabled (BP2 = 1).
  - TP3410 in the NT1 is in NT Mode.
  - The S Interface Device in the NT1 is the TP3420A.
- Command and Interrupt code points are given in Section 11 of the TP3410 datasheet.

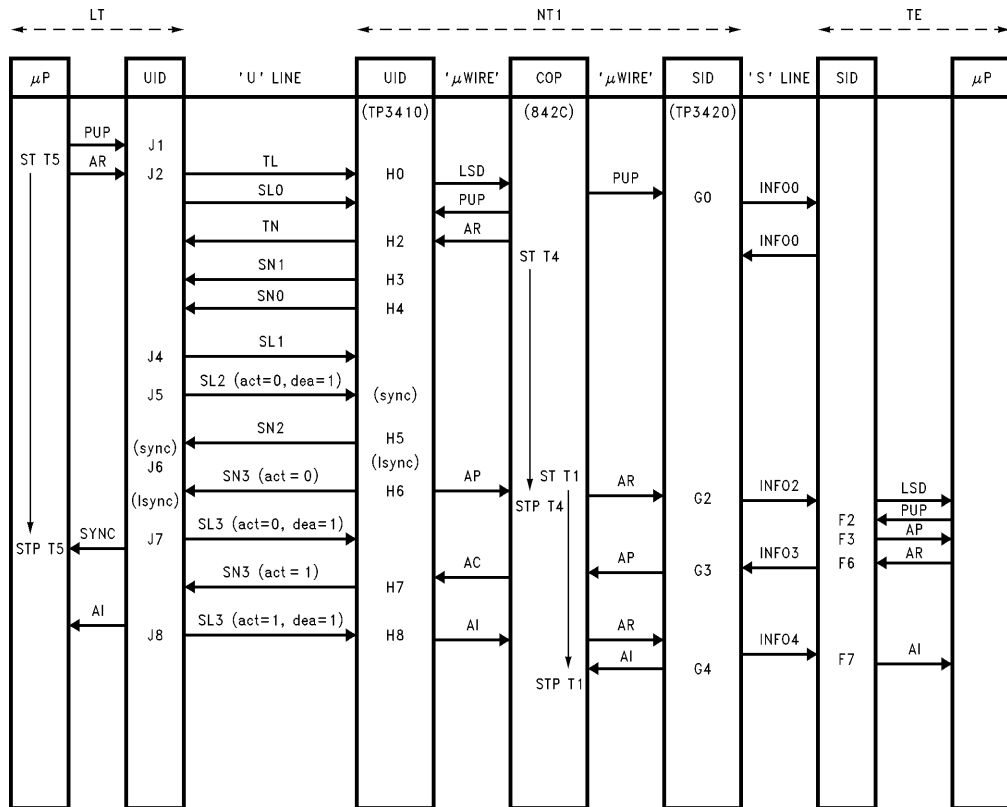
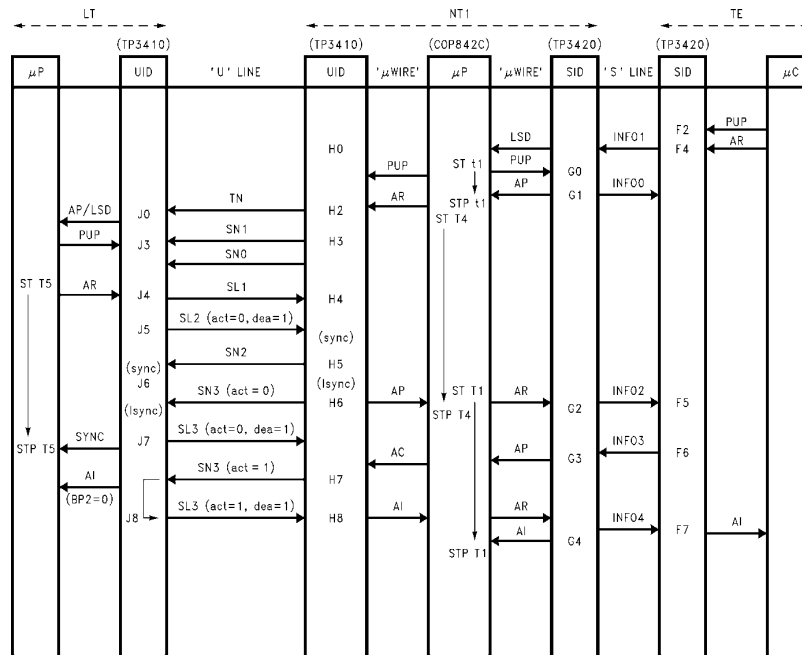
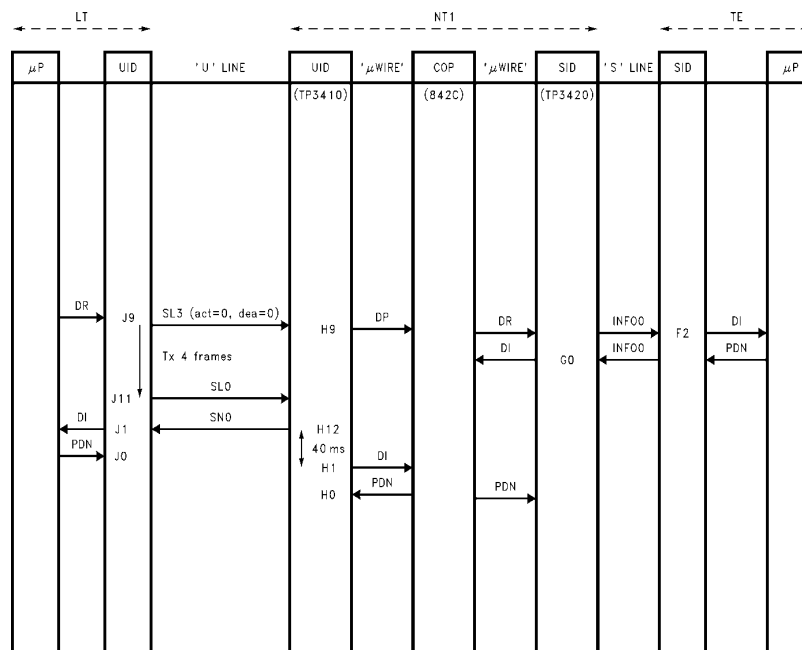


FIGURE 4. DSL Start-up Initiated by the LT

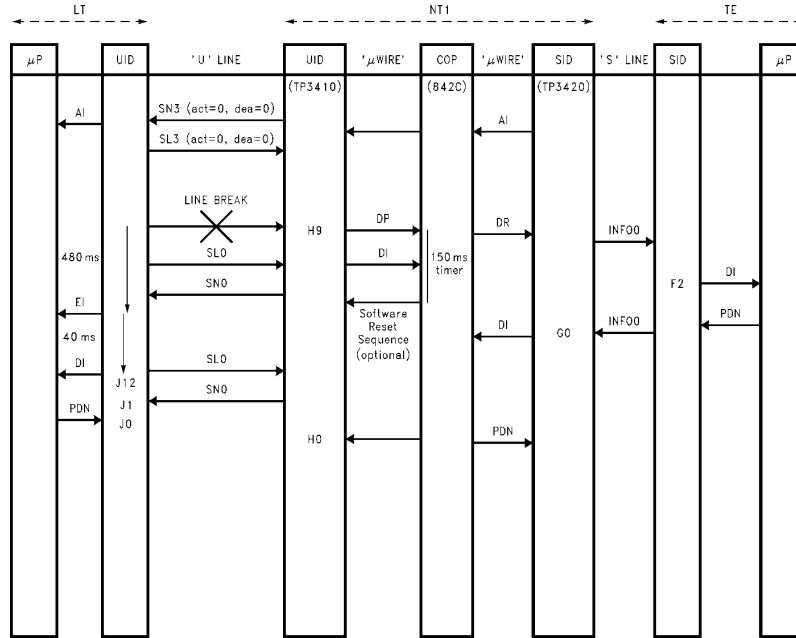
TL/H/11933-7



**FIGURE 5. DSL Start-Up Initiated by the TE**

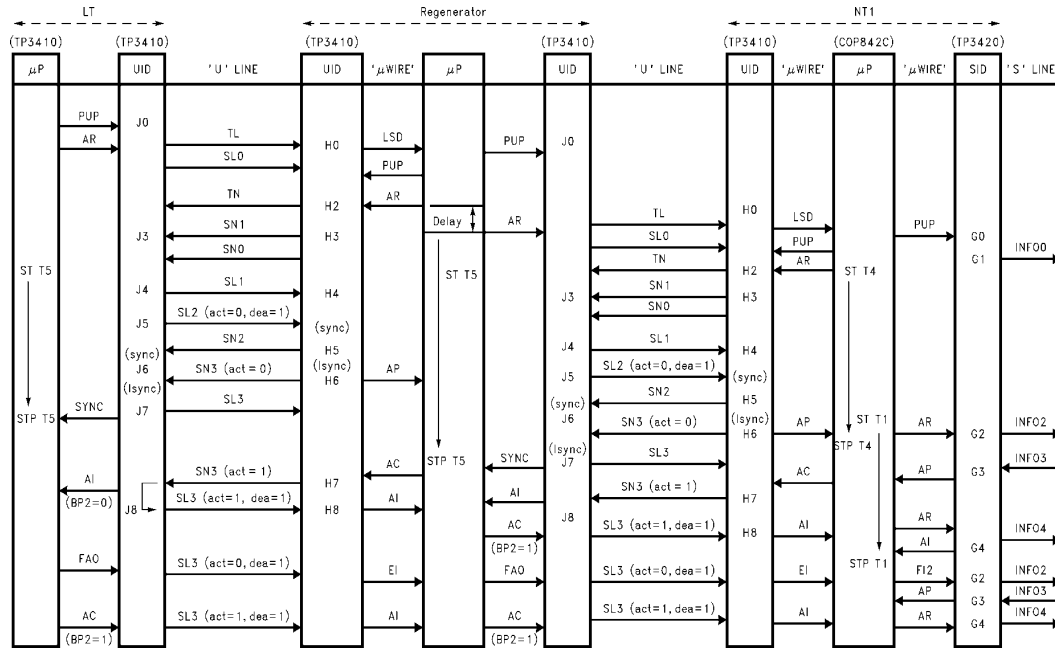


**FIGURE 6. DSL Tear-Down Initiated by the LT**



TL/H/11933-10

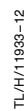
FIGURE 7. DSL Tear-Down Due to Line Break



TL/H/11933-11

**Note:** Note the Delay between the ARs for the NT and the LT ports of the regenerator. Try Delay = 2S. AR (LT port) should ideally follow AP (NT port).

FIGURE 8. Extended DSL Loop Start-Up Initiated by the LT



**FIGURE 9. Extended DSL Loop Start-Up Initiated by the TE**

## 5.0 SUPPORTING EQUIPMENT MAINTENANCE TEST MODES

### 5.1 Transmit Pulse Test Modes

After powering up the device the following transmission test modes are available:

#### Isolated +3/−3 Pulses

Writing X'1001 to the Microwire Port or GCI Monitor Channel will force the transmission of isolated +3/−3 pulses (1 single pulse/2B1Q frame) at the  $Lo\pm$  outputs, for checking against the pulse mask with the correct line interface circuit. To stop the pulses write X'1000. The Mask should be measured with the line interface circuit terminated in  $135\Omega \pm 0.1\%$ .

#### Isolated +1/−1 Pulses

Writing X'1003 to the Microwire Port or GCI Monitor Channel will force the transmission of isolated +1/−1 pulses (1 single pulse/2B1Q frame) at the  $Lo\pm$  outputs, for checking against the pulse mask (with a correctly terminated line interface circuit). To stop the pulses write X'1000.

#### Scrambled +1/−1 Pulses

Writing X'1004 to the Microwire Port or GCI Monitor Channel will force the transmission of scrambled +1/−1 pulses at the  $Lo\pm$  outputs, for comparative transmit power measurements. To stop the pulses write X'1000.

#### Scrambled +3/−3 Pulses

Writing X'1008 to the Microwire Port or GCI Monitor Channel will force the transmission of scrambled +3/−3 pulses at the  $Lo\pm$  outputs, for comparative transmit power measurements. To stop the pulses write X'1000.

### 5.2 NT1 Maintenance Modes

#### Insertion Loss Mode

The device must be powered up with a PUP command, then the command X'1804 will cause the device to continuously transmit the SN1 2B1Q line signal (2B1Q frames with no superframe syncword, and scrambled 1's in the 2B+D+M bit positions). X'1800 will stop this transmission and put the device in the reset state ready for start-up. These commands are ignored in the power-down state.

**Note:** The same command used in LT mode will cause transmission of SL1 frames, which may be useful for test purposes.

#### Quiet Mode

Several methods can be used to force the transceiver to go quiet.

1. After loop tear-down, the device may be put in PDN mode and the software programmed to ignore any LSD interrupts which may be triggered by test signals on the line. For Rev 3.3 and Rev 3.4 devices Automode should be disabled (AACT = 0 in CR4).
2. Alternatively, writing X'1880 will force the device into full reset state in which it will not generate any interrupts.

When normal operation is desired, the command X'1800 will release the reset state. **All device registers then need to be reprogrammed** to reconfigure the device back into the NT mode application.

### 5.3 Transmit 333 Hz Tone

For certain maintenance reasons, it is necessary for an NT BRITE to generate a 333 Hz tone. Rev 3.x of TP3410 has the provision to generate this tone. In CR4 (address X'2C) bit 4 (called 333 Hz) is used to control this tone. 333 Hz = 1 enables 333 Hz tone for Maintenance test modes (Bellcore requirement), 333 Hz = 0 disables it. This test tone is to be used in power up (after PUP) state but not activated. This "tone" is actually a square wave of +1/−1 values of 2B1Q as seen at the  $Lo\pm$  output pins of the device. However, due to the high pass function of the transformer, the signal at the line output appears as a square wave which is differentiated at the edges. The fundamental energy is however at 333 Hz.

## 6.0 TYPICAL APPLICATIONS

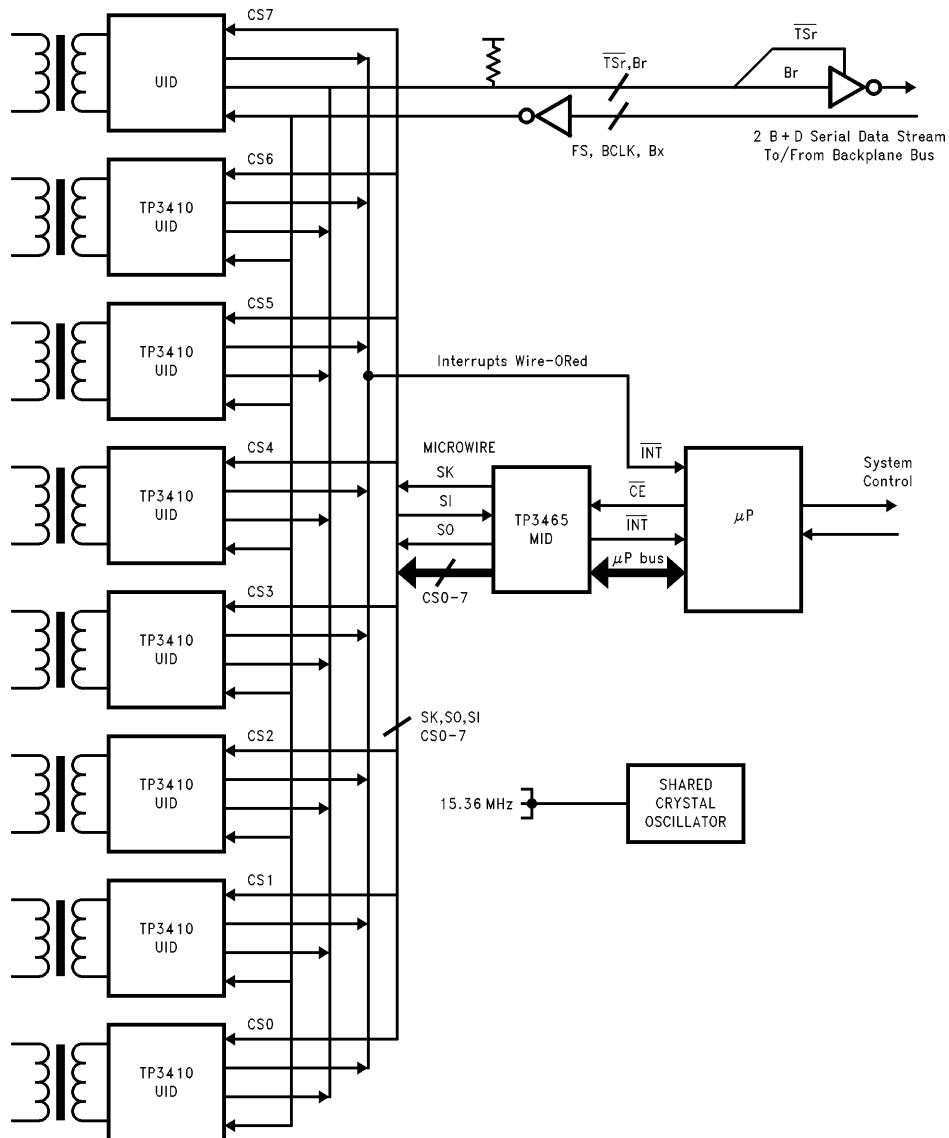
### 6.1 Octal Linecard

Figure 10 shows a linecard application using 8 TP3410s in Microwire Mode, interfacing to a Time-division Multiplexed backplane. The programmable Time-slot Assigner which is available in Format 3 is particularly useful here, since it requires only a common 8 kHz FS pulse for all channels to be distributed around the board. If required, the transmit and receive frames may be offset by using FSa for the transmit frame sync and FSb for the receive frame sync. While this application is most often used at the network end of the U interface, with the TP3410 in LT mode, it works equally well at the customer's end with the device in NT mode, for example on a PBX trunk card.

Another useful feature of the TP3410 on a line card is the freedom to share one crystal oscillator between all the channels, and to allow it to free-run relative to the backplane clocks. This is assured by a second PLL on the TP3410, which resynchronizes the internal clocks to the FSa input from the backplane when the digital interface is a slave, without "pulling" the crystal frequency.

Although the Control Interface on the TP3410 can be connected directly to the Microwire Port of any of National Semiconductor's Microcontrollers, larger line card designs often require a bus-oriented microprocessor. A new device from National, the TP3464/5 Microwire Interface Device ("MID") makes it easy to interface between 4 or 8 Microwire transceivers and a microprocessor. As shown, the MID appears to the  $\mu P$  as memory, and handles all the serial Microwire data transfers hidden from the  $\mu P$ . The TP3464 handles up to 4 Microwire peripheral devices, and the TP3465 up to 8.





TL/H/11933-13

**Note:** Using Programmable Time-slot Assignment and the TP3465 Microwire Interface Device

**FIGURE 10. Octal Linecard Application**

## 6.2 NT-1 "Core" Design

A variety of NT-1's for different applications may be based on a "core" design consisting of 3 devices, as shown in Figure 11:

1. the TP3410 U Interface Device;
2. the TP3420A S Interface Device; this is a 192 kb/s pseudo-ternary transceiver which is compliant with CCITT I.430 and ANSI T1.605-1989 for the S/T interface;
3. a COP842C 8-bit low cost Microcontroller with Microwire control interface.

To these 3 devices must be added line interface and protection circuits, which are often similar for many applications, and power supplies and supply monitors, which are tailored to the specific application, such as line-powered or locally powered. The Microcontroller connects to the 2 transceivers via their Microwire control ports, and implements the following functions in firmware:

1. top-level control of the activation procedures at both the U and the S/T interfaces;
2. 15 second default timer for U interface activation;
3. decoding of messages in the Embedded Operations Channel and executing the required commands;
4. management of the bits in the U interface M4 and spare M5/M6 fields;
5. maintenance message management for the S/T Interface S and Q channels;

6. counting and reporting of febe and nebe error-rates;
7. NT self-test sequencing.

Note that the response time required to execute these functions is relatively slow (compared with other functions in the transmission systems), making them ideally suited to a low-cost Microcontroller which can operate with low power and limited cycle times. When the 2 digital loops are deactivated, the complete NT can go into a very low power idle mode, with all 3 devices powered-down and no oscillators running. Either the far-end LT or a TE can "wake up" the NT by means of the Line Signal Detector circuits, which can reset or interrupt the COP8.

By implementing these top-level control functions in firmware rather than intergrating them onto the transceivers, 2 key advantages are gained from the Microcontroller:

1. ease of updating the design to match the requirements of future versions of the ANSI and CCITT standards, particularly for maintenance functions;
2. ability to customize the design of the NT-1 with features which differentiate the product from competing designs, such as status indicator LEDs, test modes, etc.

**Additional details for an NT1 design are covered in a separate manual called NT1 Designers Guide - Rev 2, which may be obtained from the local business center.**

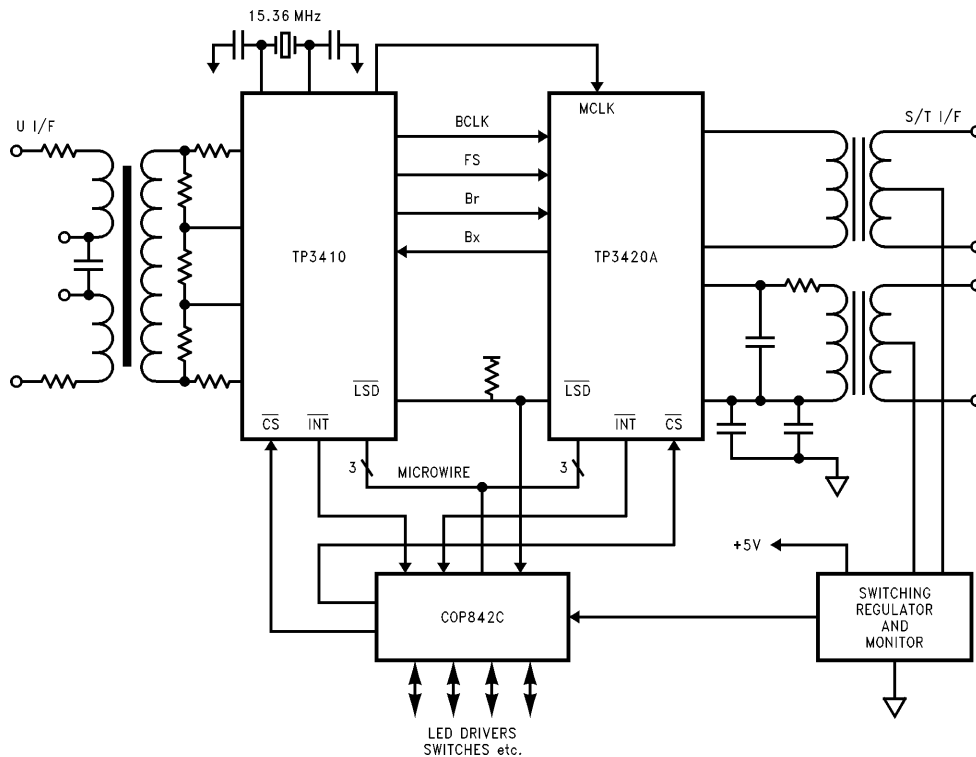


FIGURE 11. NT-1 Application

TL/H/11933-14

### 6.3 Regenerator

Figure 12 shows how a Regenerator can be built in a very similar way to the NT, to provide range extension for loops out to 24 kft and beyond.

#### 6.4 POTS Pair-Gain Application (Digital Add-On Main Line)

Applications of the 2B1Q digital loop transmission system are not limited only to true ISDN, and the flexibility of the Digital Interface timing formats, with Microwire control, make it easy to connect the B channels to various 64 kb/s peripheral devices. Figure 13 shows how the TP3410 can be used in an analog "Plain Old Telephone Set" environment. Here, the 2 "B" channels are being used to provide 2 independent 64 kb/s PCM voice channels over 1 subscriber loop pair. At the network end, the TP3410 may connect directly to the backplane in a digital switch or a DS1 terminal, using the most appropriate of the Digital Interface timing formats. Alternatively, to connect to an analog switch, each channel will require a loop termination circuit and a PCM Combo codec/filter.

#### 6.4.1 LT Master Mode

In the terminal at the network end for connection to an analog POTS interface, there is no network clock to synchronize to, and advantage can be taken of a feature of the TP3410 which allows it to operate in the LT mode but as the master of the Digital Interface timing. BCLK and FSA/b are then outputs from the device, operating synchronously with

the device 15.36 MHz oscillator, and saving the need for external counters to generate the Frame Sync signals. LT Master mode is described in the TP3410 datasheet (1992 Telecom data book). Select it by setting the CMS bit = 1 in CR1 and NTS = 0 in CR2. Also write H'1840 as part of the initialization sequence (see also Part 2.3 LT Master Mode for more details). Format 1 timing for the digital interface is probably the most useful for such an application, as it provides FSA for Combo #1 in the B1 channel, and FSb for Combo #2 in the B2 channel (transmit and receive frames tied together).

#### 6.4.2 Additional National Components for Pair-Gain Applications

In the Remote Unit at the customer's end, 2 TP3054/7 or TP3071 Combos are connected to SLICs (Subscriber Line Interface Circuits) to reconstruct the analog loops. All the functions of the Central Office Interface must also be provided, including ringing voltage generation. Loop signaling can be implemented either in-band, using robbed-bit signaling, or out-band by constructing a proprietary low speed protocol in the Microcontroller. The out-band channel might use the 2B1Q Embedded Operations Channel between the 2 terminals. Another alternative is to use the COP888CG instead of the COP822C Microcontroller; the COP888CG includes a UART which can be connected to the D channel on the TP3410, using the separate D Port option. If the HDLC protocol is preferred over a proprietary protocol, add the TP3451 HDLC controller, or use the HPC16400E Microcontroller with dual HDLCs.

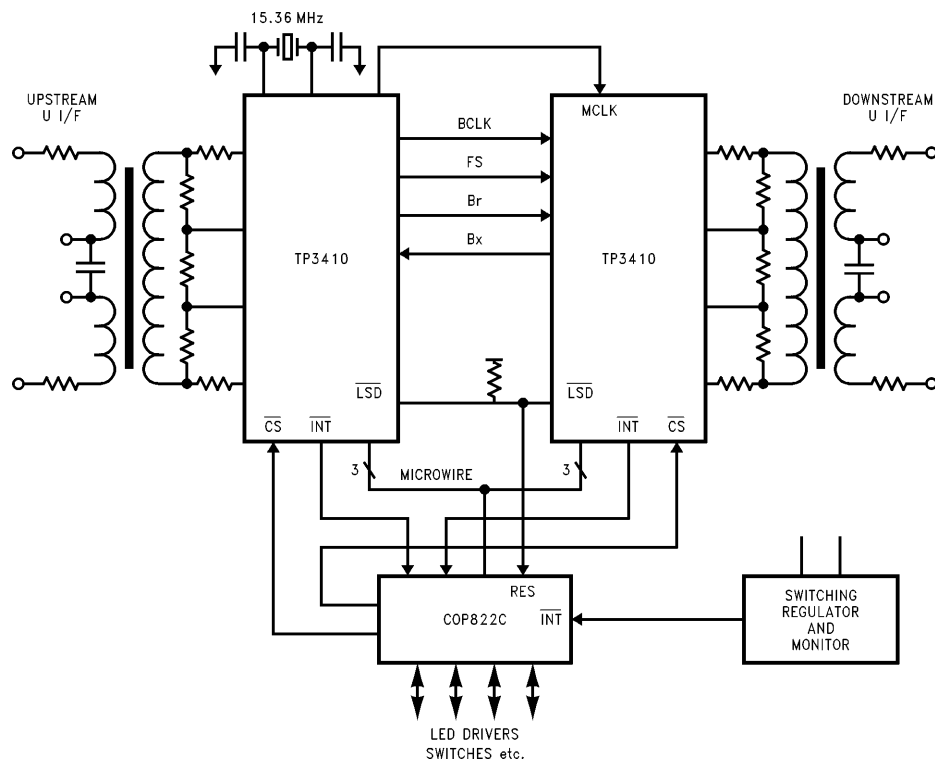
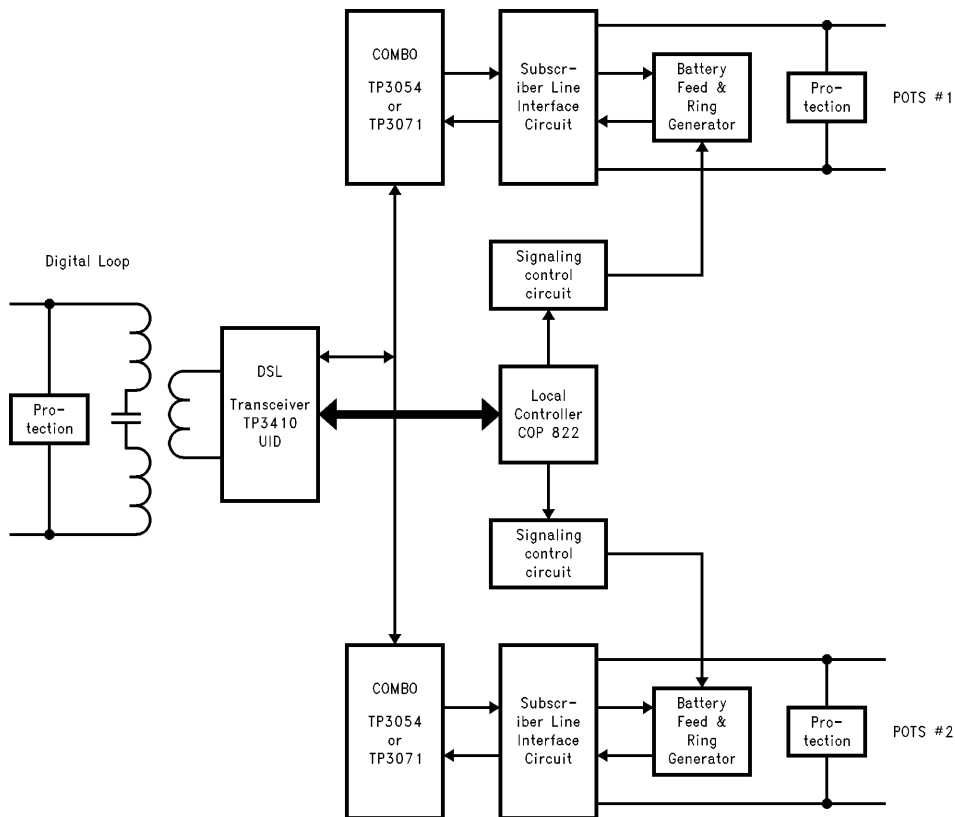


FIGURE 12. Regenerator Application

TL/H/11933-15



TL/H/11933-16

**Note 1:** Use TP3071 Combo II for Programmable Tx and Rx Gain, programmed via the microwire interface.

**Note 2:** Select Format 1, Select LT Master mode, as well as NT Master mode.

**Note 3:** TP3410 UID provides FSA for the B1 channel (transmit and receive) and FSb for the B2 channel (transmit and receive).

**Note 4:** MCLK and BCLK for the Combos can be either 1.536 or 2.048 MHz (selectable in the TP3410).

**Note 5:** National Semiconductor also offers solutions for the SLIC interface: The TP3200 MC-SLIC device family and the TP3210 SLIM family of fully integrated SLIC + Combo devices.

**FIGURE 13. POTS Pair-Gain Application**

## Part II. TP3410 Software Driver Considerations

### INDEX

- 1.0 DEVICE INITIALIZATION
  - 1.1 Full Software Reset Sequence
  - 1.2 LT Mode Initialization, Format 3
  - 1.3 LT Mode Initialization, Format 1
  - 1.4 NT Mode Initialization, Format 1
  - 1.5 List of Test Register Commands used in the Document
- 2.0 LT MODE SUBSCRIBER LOOP ACTIVATION PROCEDURES
  - 2.1 LT Loop Start-Up Procedures
    - 2.1.1 Polling for Presence of Remote NT1
    - 2.1.2 LT Auto-Activation
  - 2.2 LT Loop Tear-Down Procedures
    - 2.2.1 Loop Tear-Down for Different LT Applications
- 3.0 NT MODE SUBSCRIBER LOOP ACTIVATION PROCEDURES
  - 3.1 NT Loop Start-up Procedures
    - 3.1.1 Software Work Around for Rev 3.1 Devices
    - 3.1.2 NT Auto-Activation
  - 3.2 NT Loop Tear-Down Procedures
    - 3.2.1 Loop Tear-Down for Different LT Applications
- 4.0 OTHER TP3410 SYSTEM ISSUES AND FEATURE ENHANCEMENTS
  - 4.1 Protocol Compliance Enhancements
  - 4.2 Distinguishing Rev 3.x Devices from Rev 2.x Devices
  - 4.3 15 Second Activation Timer
  - 4.4 Dual Command PUP/DR in LT Mode
  - 4.5 LT Master Mode
  - 4.6 Auto-Activation LT or NT Modes
  - 4.7 Control of the Transmit "act" Bit in LT and NT Modes
  - 4.8 Segmented and Path Performance Monitoring
  - 4.9 Transparency of B and D Channels
  - 4.10 2B (128 kbit/s) and 2B + D (144 kbit/s) Operation
  - 4.11 Polling the Initial State of RXM4, RXM56 and RXEOC Registers
  - 4.12 LSD Noise Immunity Considerations
  - 4.13 RES Command for Cold Starts
  - 4.14 DSI SLIP Buffer
  - 4.15 Loop Tear-Down and Line Break Conditions
  - 4.16 Reading Back TP3410 Activation States
  - 4.17 Digital System Loopback Conditions
  - 4.18 RSFS Received Superframe Synch Clock
  - 4.19 NT RxEOC Control Flowchart
  - 4.20 Interworking and Data Transparency
  - 4.21 NT Software H9 State

## INTRODUCTION

This section describes firmware issues to supplement the TP3410 datasheet in the Telecom 1994 databook. The recommendations are for Rev 3.x of the TP3410.

The issues described are:

1. Loop start-up consideration for different applications
2. Loop tear-down for different applications
3. Accessing maintenance and Performance monitoring considerations
4. New features and functions added to Rev 3.x devices over those in Rev 2.8 devices.

### 1.0 DEVICE INITIALIZATION

This section discusses the initialization of the device for various configurations as well as the use of the full software reset sequence to re-establish the default state whenever necessary.

#### 1.1 Full Software Reset Sequence

The Full Software Reset sequence is used to:

- initialize the device upon first application of power;
- to reset the chip fully reset state after a fault condition such as a line break.

The reset sequence recommended for Rev 2.8 devices in earlier documentation may still be used with Rev 3.x devices, however a reduced set of instructions is all that is necessary for Rev 3.x devices. The full reset command sequence is described below:

— ***Mask out the TP3410 interrupt to the  $\mu P$  for the duration of device initialization.***

- part (a) PDN, PUP
  - part (b) X'1880, X'1800, X'100E, X'1600, X'1A00
  - part (c) Initialize all UID registers for your configuration
    - LT or NT mode
  - part (d) RES, PDN
- ***Enable the TP3410 interrupt to the  $\mu P$***

#### Notes:

Part (a):

1. PDN command is necessary to reset some portions of the internal circuitry. The PUP command provides more immunity to board noise.

Part (b):

1. For Rev 3.x devices the X'1880, X'1800, X'1000, X'1600, X'1A00 commands are used to force the device to power-on reset state.
2. To disable the internal 15s timer you can replace X'1000 by X'1002.
3. To enable the read-back of sequencer states later on, it is necessary to write X'100C. Combining this with disabling the internal 15s timer requires X'100E.
4. For LT master mode operation, write X'1840 instead of X'1800.

Part (c):

1. Initialize all the TP3410 registers for your mode of application. See following pages.

Part (d):

1. Write RES to clear LSD circuit after device initialization. A PDN can be used if power saving is required, otherwise use a PUP command to clear the RES command.

**1.2 Example of LT Mode Initialization of Registers in Format 3 with BCLK = 2048 kHz and Time-Slot Assignment Selected**

Register Name	Byte 1 Address	Byte 2 Data	Command or Function
OPR	H'20	H'1E	No interrupt if near-end crc error; no interrupt from block error counters; no interrupt if febe = 0 received; overhead bits interrupt enabled for 3x checking (RXM4 and RXM56 Registers); EOC interrupt enabled for 3x checking (RXEOC Register).
CR1	H'22	H'D0	Format 3; BCLK = 2048 kHz; DSI slave; Non-delayed data mode.
CR2	H'24	H'00	<i>LT</i> mode; D channel on Bx and Br pins; 2B + D enabled upon line sync; BP1, BP2 disabled. (if not used tie pin 22 SFS to GND).
CR4	H'2C	H'0F	standard line interface, normal mode of operation. See description for CR4.
TXB1	H'30	H'00	B1 transmit TIME SLOT = 0.
TXB2	H'32	H'01	B2 transmit TIME SLOT = 1.
RXB1	H'34	H'00	B1 receive TIME SLOT = 0.
RXB2	H'36	H'01	B2 receive TIME SLOT = 1.
TXD	H'38	H'08	D transmit TIME SLOT = 2, SUB SLOT = 0.
RXD	H'3A	H'08	D receive TIME SLOT = 2, SUB SLOT = 0.
TXM4	H'40	H'7F	Transmit M4 channel initialized.
TXM56	H'42	H'1E	Transmit M5/M6 bits initialized.
ECO1	H'46	H'FF	Block error counter 1 preset.

**1.3 Example of LT Mode Initialization of Registers in Format 1, with BCLK = 256 kHz**

Register Name	Byte 1 Address	Byte 2 Data	Command or Function
OPR	H'20	H'1E	No interrupt if near-end crc error; no interrupt from block error counters; no interrupt if febe = 0 received; overhead bits interrupt enabled for 3x checking (RXM4 and RXM56 Registers); EOC interrupt enabled for 3x checking (RXEOC Register).
CR1	H'22	H'00	Format 1; BCLK = 256 kHz; DSI slave; non-delayed data mode.
CR2	H'24	H'00	<i>LT</i> mode; D channel on Bx and Br pins; 2B + D enabled upon line sync; BP1, BP2 disabled. (if not used tie pin 22 SFS to GND).
CR3	H'26	H'00	No loopbacks in effect.
CR4	H'2C	H'0F	Standard line interface, normal mode of operation. See description for CR4.
TXM4	H'40	H'7F	Transmit M4 channel initialized.
TXM56	H'42	H'1E	Transmit M5/M6 bits initialized.
ECO1	H'46	H'FF	Block error counter 1 preset.

**1.4 Example of NT Mode Initialization of Registers in Format 1, with BCLK = 256 kHz**

Register Name	Byte 1 Address	Byte 2 Data	Command or Function
OPR	H'20	H'1E	No interrupt if near-end crc error; no interrupt from block error counters; no interrupt if febe = 0 received; overhead bits interrupt enabled for 3x checking (RXM4 and RXM56 Registers); EOC interrupt enabled for 3x checking (RXEOC Register).
CR1	H'22	H'02	Format 1; BCLK = 256 kHz; DSI Master; non-delayed data mode.
CR2	H'24	H'40	<i>NT</i> mode; D channel on Bx and Br pins; 2B + D enabled upon line sync.
CR3	H'26	H'00	No loopbacks in effect.
CR4	H'2C	H'0F	Standard line interface, normal mode of operation. See description for CR4.
TXM4	H'40	H'7F	Transmit M4 channel initialized.
TXM56	H'42	H'1E	Transmit M5/M6 bits initialized.
ECO1	H'46	H'FF	Block error counter 1 preset.

### 1.5 List of Test Register Commands Used in the Document

There are 8 additional test registers not described in the data sheet. These are registers TRG0 through TRG7 located at address X'10, X'12, X'14, X'16, X'18, X'1A, X'1C, X'1E.

The registers may be read by using the odd addresses, X'11, X'13, X'15, X'17, X'19, X'1B, X'1D, X'1F.

Specific device features/functions can be exercised via these registers and this list is provided below. Only a very few of these are ever necessary for Rev 3.x devices.

- X'1000 — Clear Register at address X'10, hence stop conditions controlled by this register (TRG0—Test Register 0)
- X'1002 — Disable internal 15s timer (Part II, Section 1.1)
- X'100C — Enable read-back of internal sequencer states (Part II, Section 4.16)
- X'100E — Disable internal 15s timer and enable read-back of internal states (Part II, Section 1.1)
- X'1001 — Transmit isolated +3/−3 pulses
- X'1003 — Transmit isolated +1/−1 pulsed
- X'1004 — Transmit scrambled +1/−1 levels of 2B1Q
- X'1008 — Transmit scrambled +3/−3 levels of 2B1Q
- X'1200 — Clear Registers at address X'12 (TRG1—Test Register 1)
- X'121F — Set NR = 0.0 (NR—Noise Reduction Filter to reduce gaussian noise)
- X'123F — Set NR = 0.25
- X'125F — Set NR = 0.5
- X'127F — Set NR = 0.125
- X'1400 — Clear Register at address X'14 (TRG2—Test Register 2)
- X'14C9 — Set convergence parameter to 2–15
- X'1600 — Clear Register at address X'16, hence stop conditions controlled by this register (TRG3—Test Register 3)
- X'1608 — Enables control of transmit “act”, “dea” bits via TXM4 register
- X'1610 — Forces transparency of 2B + D channels
- X'16C4 — Power-up device in case of lock-up condition
- X'1800 — Clear register at address X'18, hence stop conditions controlled by this register (TRG4—Test Register 4)
- X'1880 — Force device reset
- X'1840 — Bypass PLL1 for LT master mode operation
- X'1804 — Transmit scrambled 2B1Q pattern continuously (SN1–NT mode, SL1–LT mode). Can be used for Test purposes
- X'1A00 — Clear Register at address X'1A, hence stop conditions controlled by this register (TRG5—Test Register 5)
- X'1A08 — Forces internal signal energy detector to be squelched, forcing internal loss of signal to be triggered after 3 ms. This can be used to deliberately deactivate the device
- X'1A20 — Inhibit internal convergence sequencer to allow external forcing of convergence parameters
- X'1A40 — Freeze PLL2 in LT mode (Rev 3.2, 3.3 and 3.4). X'1A00 to return to normal

- X'1C00 — Clear Register at address X'1C (TRG6—Test Register 6)
- X'1C04 — Force RSFS signal on pin 25 (must also have X'100C or X'100E)
- X'1C2B — Normal state for activated Rev 3.x devices
- X'1C0B — Freeze PLL2 (use after X'1A20)
- X'1C2A — Freeze PLL1 integrator (use after X'1A20)
- X'1E00 — Reset this register to default states (TRG7—Test Register 7)
- X'1E48 — Reset Line Signal Detect (LSD) analog circuit
- X'1E60 — Force internal convergence parameter

### 2.0 LT MODE SUBSCRIBER LOOP ACTIVATION PROCEDURES

This section deals with subscriber loop start-up and tear-down procedures while the device is working in LT mode, as in LT linecard, or LULT or a COT equipment.

#### 2.1 LT Loop Start-Up Procedures

This section recommends software actions to activate (start-up) a Digital Subscriber Loop DSL using a TP3410 operating in LT mode. Normally, DSL start-up is initiated from the LT end, and hence the NT mode equipment responds to loop start-up sequences from the LT. The only exception is for an NT1 product in North America; when it is first installed, it may make one attempt to perform loop start-up procedures per ANSI T1.601-1991.

Loop start-up or activation may be started from the local (or near end) or remotely (or far end). In the power-down state, the TN tone (10 kHz) from the NT will cause the LSD pin to be pulled low (this may be used to wake up the microprocessor), and the AP interrupt to be generated.

The example below assumes that the device was initialized with the following:

- X'100E disable internal timer and enable read-back of activation states.
- BP2 = 1 in CR2 register, to enable activation breakpoint.
- DD = 0 in CR2 register (control of DD is now optional—see Section 4.9).

#### FOR LOCAL ACTIVATION

##### When ready to commence activation:

- Write PUP to power-up the chip.
- Wait 15 ms to allow internal circuits to settle.
- Jump to Start activation sequences.

#### FOR REMOTE ACTIVATION

##### Actions after AP interrupt:

The AP interrupt in LT mode indicates 10 kHz wake-up tone TN from far end is detected.

- Jump to Start activation sequences.

##### Start activation:

- Write PUP.
- Write AR to commence activation (must occur within 6 ms of AP).
- Start T5 (15s timer).

##### Actions after SYNC interrupt:

- Stop the timer T5 as superframe synchronization has been achieved.

- If BP2 = 1 then write AC to complete activation. If BP2 = 0, device proceeds automatically.

#### Actions after AI interrupt:

- On first occurrence of AI: Full end-to-end transparency achieved.
- Subsequent occurrences of AI may be ignored until the chip is deactivated following a DI interrupt, or is fully reset. Multiple AI's may occur during a line break due to transients on the line causing the "act" bit to toggle. The exception is in products such LULT and Repeater where the "act" bit (and hence the AI interrupt) is deliberately controlled after loop synchronization by means of the FAO and AC commands (with BP2 = 1), see Section 4.7.

#### Action if T5 timer expires:

- Activation has failed, Reset the chip by **either** writing RES command **or** write full software reset sequence (Section 1.1).

#### 2.1.1 LT Application: Polling for Presence of NT1

For Rev 3.x devices, while initiating activation from LT mode, if there is no NT present at the remote end, the LT device sends the TL tone and then waits until the 15 second timer expires. This is a correction/enhancement to Rev 2.x devices for which the LT would continue to send SL1, SL2 until the timer expired even though there was no NT at the far end.

If desired it is possible to reduce the 15 second timer duration between LT initiated activation attempts. The procedure is described below:

Start a 3 second timer after writing AR to start activation from the LT end. When this 3 second timer expires, read back the state of the LT device by writing X'1B00.

If the device state is J3 (X'1Bx7—state tables in section 4.16) then it is waiting for a non-existent NT. The RES command can be used to reset the chip and a re-attempt at activation can be made. (Remember to send either the PDN or PUP command after DI.) This allows activation attempts at every 3 seconds or so.

If the LT state has proceeded beyond J3, (i.e. J4 or J5) then a timer may be restarted to count 12 seconds, for the remainder of the 15 seconds, or let the internal timer take over the control of the activation time (if enabled during device initialization).

#### 2.1.2 Auto-Activation LT

In Rev 3.2 device, a new function is being introduced to enable auto-activation. This function is controlled by the AACT bit 6 in CR4 register.

**AACT** Auto-Activation control. AACT = 1 enables auto-activation in either LT or NT modes. AACT = 0 disables it (default state) and the device behaves normally. The LT has to respond before the end of the incoming TN tone (9 ms duration). Allowing for device circuit delays, the software has about 5 ms to respond to the AP (line signal detect) interrupt with PUP and AR. This is normally no problem where a single LT device is controlled by a single processor. If however, if a single processor controls multiple LT devices, it is desirable to allow the device to respond to the TN tone by powering itself up and setting the AR condition. This auto-activation feature is invoked by the AACT bit. Even

though the device responds to TN automatically, it is still possible to write a PUP and AR commands (without upsetting anything) to maintain similarity of the code for local or remote activations. **This function is available in TP3410 Rev 3.3 and 3.4 devices.**

#### 2.2 LT Mode Loop Tear-Down Considerations

This section recommends software actions to be taken after receiving deactivation/loop tear-down related interrupts from the TP3410 operating in the LT mode.

##### Actions after EI interrupt:

EI interrupt is caused by either (i) loss of synch for > 480 ms (ii) loss of signal for > 480 ms or (iii) receiving "act" = 0, and causing a state transition from J8 to J7.

Transition from J8 to J7 state may be confirmed by reading back the device state: write X'1B00 and wait for the read-back interrupt. If the read-back indicates X'1BxD, the device is in the J7 state. After the 480 ms time of qualifying loss of synch or loss of signal, the 2B + D data stream on pin Br is inhibited (forced to 1-tristate).

For whatever the cause of EI, it may be necessary to perform an action depending on the application.

- If the product is an LT linecard, the S/T interface loop has lost data transparency.
- If the product is an LULT card, the S/T interface loop has lost data transparency, so send the "act" = 0 condition upstream to the LUNT and towards the central office.

##### Actions after DI interrupt:

There are three alternatives:

##### a. To allow warm starts when possible:

- Write PDN to enter low power mode (or a PUP command to stay in power up mode)
- Reset all software Flags and software counters.

##### or b. To force cold start and to clear any spurious LSD interrupt:

- Write RES, PDN (or PUP if staying in PUP state)
- Reset all software Flags and software counters.

##### or c. To re-start from initialized state:

- Write the Full Software Reset Sequence
- Reset all software Flags and software counters.

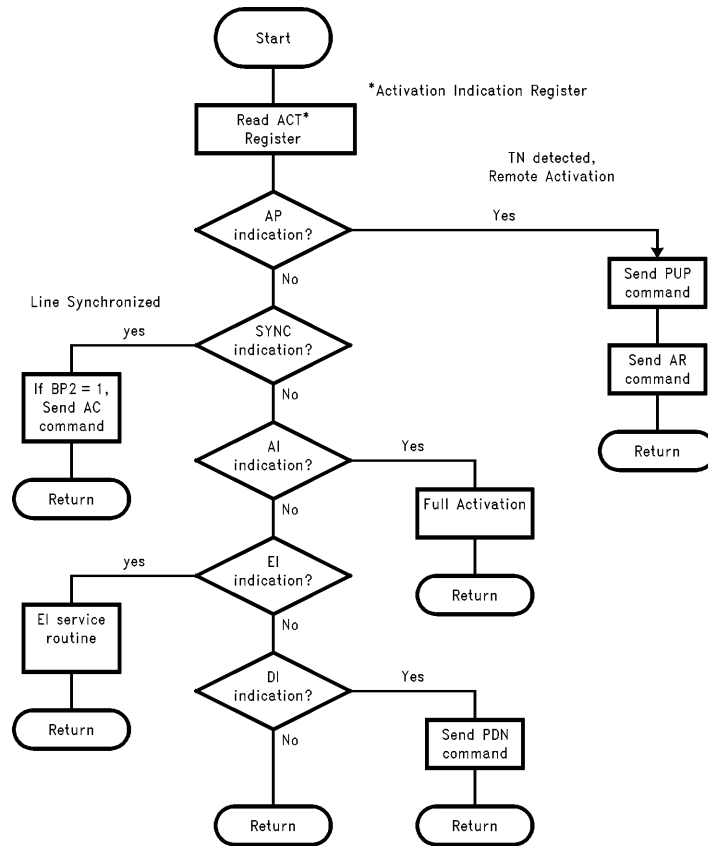
#### 2.2.1 Loop Tear-Down for Different LT Mode Applications

##### Repeaters, Line Cards, COT

For Repeater applications, power is typically fed from the Central Office end, and the Repeater contains both an NT mode device and an LT mode device. Loop tear-down/deactivation generally results from a line-break, which also removes power to the Repeater. The LT mode device in linecards, COTs and LULT is normally powered all the time.

The device handles line break conditions and recovers to the reset state by itself. The full software reset sequence may be used to restore the device to initialized state. This is however not necessary as an irregular deactivation (such as a line-break) will cause the device to attempt a cold start activation the next time.

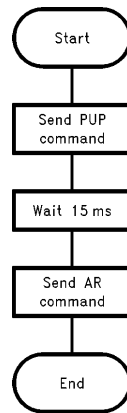




TL/H/11933-17

**Note:** Please see section 2 of this manual for additional software considerations for device driver design.

**ACT Register Interrupt Service Routine Flow Chart: LT Mode Example**



TL/H/11933-18

**Local Activation Sequence: LT Mode Example**

### 3.0 NT MODE LOOP SUBSCRIBER LOOP ACTIVATION PROCEDURES

This section deals with subscriber loop start-up and tear-down procedures while the device is working in NT mode, as in NT1, LUNT, and NT1 + TE combination on user premises.

#### 3.1 NT Mode Loop Start-Up Procedures

This section recommends software actions to activate (start-up) a Digital Subscriber Loop (DSL) using a TP3410 operating in NT mode. Normally, a DSL start-up is initiated from the LT end and hence the NT mode equipment responds to loop start-up sequences from the LT. One exception is for an NT1 product in North America; when it is first installed, it may make one attempt to start-up the DSL, per ANSI T1.601-1991.

Loop start-up or activation may be started from the local (or near end) or remotely (or far end). In the power-down state, the TL tone (10 kHz) from the LT will cause the LSD pin to be pulled low (this may be used to wake up the microprocessor), and the LSD interrupt to be generated.

The example below assumes that the device was initialized with the following:

- X'100E disable internal timer and enable read-back of activation states.
- DD = 0 in CR2 register (control of DD is now optional—see Section 4.9).

#### FOR LOCAL ACTIVATION:

##### When ready:

(in an NT1 product, this may be when power is first applied to the equipment),

- Jump to Start activation sequences.

#### FOR REMOTE ACTIVATION:

##### Actions after LSD interrupt:

The LSD interrupt in NT mode indicates 10 kHz wake-up tone from far end is detected.

- Jump to Start activation sequences.

##### Start activation:

- Write PUP to power up the chip if not already in PUP mode.
- Write AR (within 0.5 ms of receiving LSD interrupt) to commence activation. Start T4 (15s timer).

##### Actions after AP interrupt:

- Stop the timer T4 as superframe synchronization has been achieved.
- Write AC command to continue activation. (see Section 3.1.3 for additional considerations)

##### Actions after AI interrupt:

- On first occurrence of AI: Transparency of data is achieved.
- Subsequent occurrence of AI may be ignored until the chip is deactivated following a DI interrupt, or is fully reset. Multiple AI's may result from a line break due to transients on the line causing the "act" bit to toggle. The exception is in products such LUNT and Repeater where the "act" bit (and hence the AI interrupt) is deliberately controlled after loop synchronization by means of the FAO and AC commands at the LT end (see Section 4.7).

#### Action if T4 timer expires:

- The activation attempt has failed, so reset the chip by writing **either** RES command **or** Perform the full software reset (section 1.1).

#### 3.1.1 Software Work-Around (Rev 3.1) Required for Certain NT Applications

A software change **may** be required for NT1 and LUNT applications to cope with all conditions of operation. In NT mode, if the device stays in H6 state (acquired synchronization but not fully activated with "act" = 1 set for both sides) for a long period of time (greater than 5 minutes), it is possible that the device will deactivate by itself. To prevent this from happening, it is necessary to perform the following **additional** steps in the software.

**After AP (NT mode) write : X'1A20, X'123F, X'1455**

**After AI, and EI and DP, write X'1A00** to restore the hardware control of the sequencer.

**After DI, write X'1A00, Delay 5 ms PDN (PUP)**

These steps should allow the system to work all cases of NT operation. **This work-around is not to be required for the Rev 3.2 of the part. Rev 3.1 will not be released to production.**

#### 3.1.2 Auto-Activation NT

In Rev 3.3 device, a new function is being introduced to enable auto-activation. This function is controlled by the AACT bit 6 in CR4 register.

**AACT** Auto-Activation control. AACT = 1 enables auto-activation in NT modes. AACT = 0 disables it (default state) and the device behaves normally. The NT has to respond before the end of the incoming 3 ms TL tone. Allowing for device circuit delays, the software has about 0.5 ms to respond to the LSD interrupt with PUP and AR. This is normally no problem where a single NT device is controlled by a single processor. If however, if a single processor controls multiple NT devices, it is desirable to allow the device to respond to the TL tone by powering itself up and setting the AR condition. This auto-activation feature is invoked by the AACT bit. Even though the device responds to the TL automatically, it is still possible to write a PUP and AR commands (without upsetting anything) to maintain similarity of the code for local or remote activations.

**This function is available in Rev 3.3 and 3.4 devices.**

#### 3.1.3 Limitation of Rev 3.2 Devices While in H6 State in NT Mode

Recent tests have uncovered a limitation in the Rev 3.2 devices while operating in NT mode and in H6 state during a cold start. While in the H6 state, the devices do not report any received M4, M56 or EOC messages. This limitation is only apparent if the equipment stays in the H6 state on the first start-up condition as in the case of an NT1 with no S Terminal plugged-in.

**Work-Around:** Force the NT device to transition through the H6 state on to H7 by responding to the **AP interrupt** with:

**AC (X'440C), Delay (5 ms), SEI (X'4404)**

This forces the device to transition to H11 state. While in H11 state, the device will receive EOC, M4 and M56 messages.

External signals as well as state transition conditions for the H11 state are identical to that of H6. A subsequent AC command (when the S interface receives info 3) will cause the device to transition to H7 and send out “act” = 1 towards the LT.

**This work-around forces the device in a valid state H11 (waiting for the S interface to be synchronized), and will work for all applications, and even for prior design using Rev 2.8 devices.**

### 3.2 NT MODE LOOP TEAR-DOWN CONSIDERATIONS

This section recommends software actions to be taken after receiving deactivation related interrupts from the TP3410 operating in the NT mode.

#### Actions after DP interrupt:

- Ignore any RXM4, RXM56 or any additional LSD/DP interrupts.

#### Actions after EI interrupt:

EI interrupt is caused by either (i) loss of synch for > 480 ms (ii) loss of signal for > 480 ms or (iii) receiving “act” = 0, and causing a state of transition from H8 to H7.

Transition from H8 to H7 state may be confirmed by reading back the device state: write X’1B00 and wait for the read-back interrupt. If the read-back indicates X’1BxD, the device is in the H7 state. After the 480 ms time of qualifying loss of synch or loss of signal, the 2B + D data stream on pin Br is inhibited (forced to 1-tristate).

For whatever the cause of EI, it may be necessary to perform an action depending on the application.

- In an NT1 product, partially deactivate the S/T interface loop by writing FAO to the TP3420A SID transceiver.
- In a LUNT product, send the “act” = 0 information downstream to the LULT via the T1 interface (or equivalent).
- For TE + NT1 application, the EI interrupt would indicate that data transparency is blocked.

#### Actions after DI interrupt:

Perform one of the following three sequences:

##### a. To allow warm starts when possible:

- Write PDN to enter low power mode (or a PUP command to stay in power up mode)
- Reset all software Flags and software counters.

##### or b. To force cold start and to clear any spurious LSD condition:

- Write RES, PDN (or PUP if staying in PUP state)
- Reset all software Flags and software counters.

##### or c. To re-start from initialized state:

- Write the Full Software Reset Sequence (Section 1.1)
- Reset all software Flags and software counters.

### 3.2.1 Loop Tear-Down for Different NT Mode Applications

#### Line-Powered Applications, such as Analog Pair-Gain (DAML), UDC (Bellcore TR-000398), NT’s and Repeaters which Cold-Start Only.

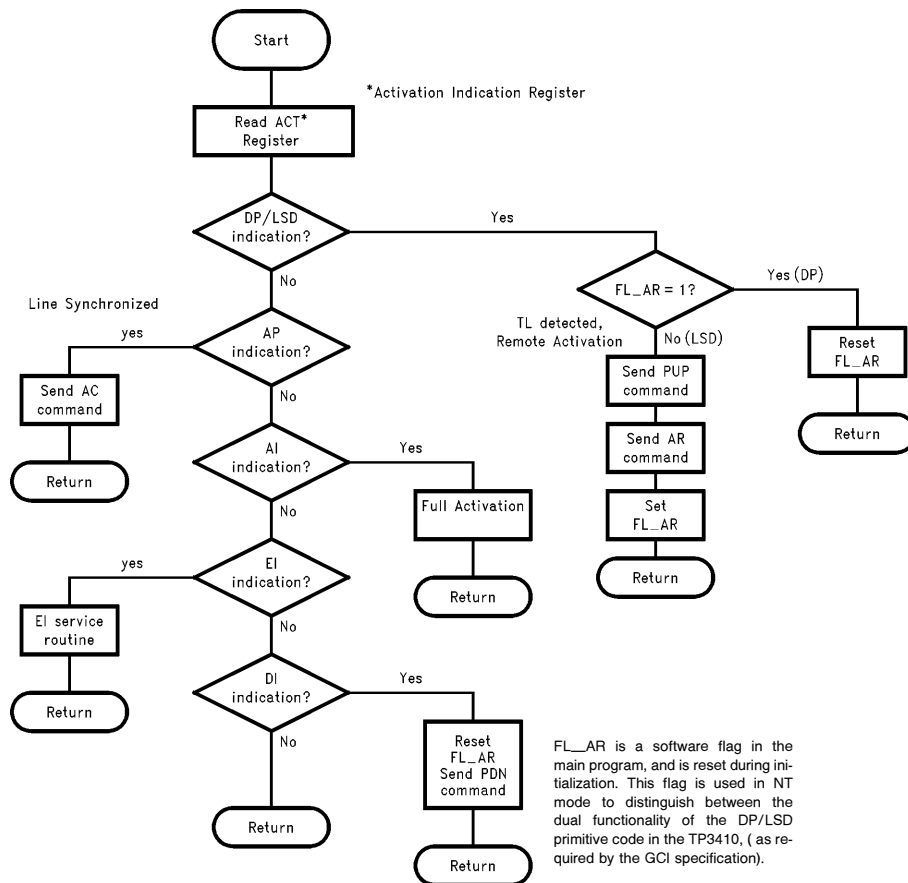
In these applications power is fed from the LT end, and Loop tear-down/deactivation typically does not use the specified deactivation procedures. Thus tear-down occurs only as a result of a line-break, which also removes power to the NT mode device.

In Europe, the DSL will make use of warm-start activations on a per-call basis, which is accommodated in the steps for loop tear-down interrupt servicing as outlined above.

#### Locally Powered NT’s, Data Communication Applications of UDC (Bellcore TR-000398) and UDLC Applications in LUNT (Bellcore TR-000397).

In these applications, if the NT end is locally powered a line-break does not guarantee loss of power to the NT mode chip to bring it back to the reset state.

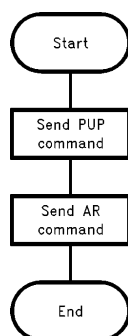
The device handles line-break conditions and recovers to the reset state by itself. The full software reset sequence may be used to restore the device to initialized state. This is, however, not necessary as an irregular deactivation (such as a line-break) will cause the device to attempt a cold start activation the next time.



TL/H/11933-19

**Note:** Please see section 3 for additional software considerations for device driver design.

#### ACT Register Interrupt Service Routine Flow Chart: NT Mode Example



TL/H/11933-20

#### Local Activation Sequence: NT Mode Example

#### 4.0 OTHER TP3410 SYSTEM ISSUES AND FEATURE ENHANCEMENTS

##### 4.1 Protocol Compliance Enhancements

The following enhancements have been implemented in the Rev 3.x device to comply with the newer ANSI T1-601 specification:

1. In NT mode, SN2 is delayed until SL2 from LT is detected (H4 to H6 transition).
2. While in NT mode, the H6 state data transparency is blocked as required by ANSI 601.
3. LT will not transmit SL1 if there is no NT at the far end. The LT end device will stay quiet and can be reset with RES command after the expiry of external 15s timer. If internal 15s timer is invoked, the device will return to the reset state after the timer expires.

##### 4.2 Distinguishing Rev 3.x from Rev 2.x Device

Configuration Register 4 (CR4) has been added to Rev 3.x devices and this can be used as a distinguishing feature. The CR4 does not exist in Rev 2.8 and hence the value read back from this register location will be random. The procedure is as follows:

Write to CR4 X'FA i.e. write X'2CFA

Write to CR3 X'55 i.e. write X'2655

Read back CR4 i.e. write X'2D00,

and check the register content (byte 2) after read back interrupt and interpret as follows:

X'1A —this device is Rev 3.1

X'7A —this device is Rev 3.2

X'FA —this device is Rev 3.3 or Rev 3.4

else —this device is Rev 2.x

Restore CR4 to X'0F (default state) by writing X'2C0F.

##### 4.3 15 Second Activation Timer

###### Rev 3.x Devices

For Rev 3.x devices, the 15s internal timer is enabled as a power-up default condition. The timer is automatically started with the AR command, and is stopped if the device gets to state H6 (NT mode) or J7 (LT mode) for a successful activation. If the timer expires before reaching the H6 or J7 states, the device generates the EI interrupt followed (about 45 ms later) by a DI interrupt. After DI, the device is returned to H1 or J1 (reset) state.

Note that in LT mode, if there is no response from the NT at the far end, the first indication to the LT controller occurs when the 15s timer expires and the device generates the EI/DI interrupts. However, in the NT mode, if there is no response from the LT at the far end, the EI/DI interrupts will occur much earlier—within 1s of initiating activation from the NT end—well before the expiry of the 15s timer.

Optionally, if an external software timer is preferred, the **internal timer may be disabled** by writing X'1002. It can be re-enabled with X'1000. On the expiry of the software timer, there are two options for resetting the chip to attempt another activation:

- (i) Use the RES command and wait for the DI interrupt before re-attempting activation (Rev 3.x devices).
- (ii) Alternatively issue the full software reset sequence to restore the device to reset state to re-attempt activation.

##### 4.4 Dual Command PUP/DR in LT Mode

In the LT mode the Power-up and Deactivate Request commands PUP/DR have the same code X'4400. The X'4400 is treated as a PUP command prior to an AR command and thereafter, the X'4400 is treated as a DR command.

##### 4.5 LT Master Mode

For certain applications (Analog Main Line—AML, Data Analog Main Line—DAML, Baseband MODEM applications, etc.), the central office derived clock is not available and the LT mode device needs to generate the system clocks (8 kHz—FS, and BCLK, etc.) from a free running master clock of 15.36 MHz. The TP3410 UID supports this function.

**Set the CMS bit in the CR1 register. Write X'1840 as part of the UID initialization procedure.**

This will cause the LT mode device to derive the FS (8 kHz) and the BCLK (frequency selectable) from the MCLK master clock and bypass the internal phase lock loop circuit (PLL1) which is normally used to synchronize the internal clock to the 8 kHz backplane clock. With these settings the Rev 3.x device performs reliable and repeatable cold start or warm start loop activations and deactivations.

##### 4.6 Auto-Activation LT or NT

In Rev 3.3 and 3.4 devices, a new function is provided to enable auto-activation. This function is controlled by the AACT bit 6 in CR4 register. See Section 9.6 of the TP3410 1994 datasheet for a full CR4 description.

**AACT** Auto-Activation control. AACT = 1 enables auto-activation in either LT or NT modes. AACT = 0 disables it (default state) and the device behaves normally. The LT has to respond before the end of the incoming TN tone (9 ms duration). Allowing for device circuit delays, the software has about 5 ms to respond to the AP (line signal detect) interrupt with PUP and AR. This is normally no problem where a single LT device is controlled by a single processor. If however, if a single processor controls multiple LT devices, it is desirable to allow the device to respond to the TN tone by powering itself up and setting the AR condition. This auto-activation feature is invoked by the AACT bit. Even though the device responds to the TN automatically, it is still possible to write a PUP and AR commands (without upsetting anything) to maintain similarity of the code for local or remote activations.

This bit also performs a similar auto-activation function in NT mode, although this may not be used often.

**This function is available in Rev 3.3 and 3.4 devices.**

##### 4.7 Control of the Transmit “act” Bit in LT and NT Modes

The state of the “act” bit may be used to control transparency of the data path all the way from the LT to the Terminal. The device in LT mode ( ) automatically controls the state of the “act” bit during activation and deactivation. After reaching the activated state AI (“act” is set to 1), software control of the “act” bit may be done as follows:

###### LT Mode:

Set BP2 = 1 in CR2 to enable control of the transmit “act” bit, then

— to force the transmit “act” = 0, write FAO (X'4404)

— to force it back to “act” = 1, (with BP2 = 1 in CR2 register) write AC (X'440C)

#### NT Mode:

To reflect the activation status of the S interface, it is necessary to control the “act” bit sent to the network.

- Write SEI command (X’4404), to force the transmit “act” = 0.
- Write AC command (X’440C) to set transmit “act” = 1

#### 4.8 Segmented and Path Performance Monitoring

In certain applications (Universal Digital Carrier—UDC, etc.) it is necessary to control the “febe” bit downstream back to the LT by software depending on the condition from the upstream links.

The outgoing “febe” bit from the NT mode device is normally controlled by the device itself; it is set to 0 when the received CRC is incorrect (the device also generates a “nebe” interrupt locally if enabled).

Rev 3.x devices contain a very flexible control of the outgoing febe bit to support Segmented and Path Performance Monitoring recommendations in Bellcore TR 397. This is achieved via three control bits LFS, RFS and TFB0 in new register CR4.

For Rev 2.8 compatible operation, set RFS = 1, LFS = 1 and TFB0 = 1 (these are the power up default settings). This setting will cause the transmit febe to be computed as OR of the incoming nebe bit and the state of the TFB bit in TXM56 (representing the adjacent section febe to be forwarded).

**LFS** Local Febe select, LFS = 1 (default state) the state of the outgoing febe bit is computed using the incoming nebe bit. If LFS = 0, the outgoing febe is not dependent on the incoming nebe.

**RFS** Remote Febe select, RFS = 1 (default state), the state of the outgoing bit is computed based on the state of the TFB (bit 1) in TXM56 register. The TFB bit is set = 0 by the software to allow a febe bit from an adjacent DSL to be forwarded to the next section in the next superframe. This bit is self resetting (to 1) in rev 3.x devices. This is a change from the Rev 2.x devices. If RFS = 0, then the outgoing febe does not depend on the state of the TFB bit in TXM56 register.

**TFB0** TFB0 = 0 forces transmit febe to 0 continuously for test purposes. TFB0 = 1 (default state) allows normal operation controlled by LFS and RFS. Note that this function was controlled by the TFB bit in TXM56 register in Rev 2.x devices. The TFB bit in TXM56 bit is now (Rev 3.x) active for one superframe only; if set to 0 by software, a superframe will transmit febe = 0, and then the TFB will be reset to 1 by the device, the software does not need to set it to 1.

#### 4.9 Transparency of B and D Channels

The TP3410 Rev 3.x device controls data path transparency during start-up sequence according to the T1.601 specification.

**NT Mode Requirement:** During the activation sequence the Rev 3.x device in NT mode sends scrambled “1s” until it reaches states H7 or H8. The device then transparently sends Bx data to the line during the late activation stages (H7, H8, H9, H11 only). Similarly the line input data is sent out to Br pin in the same states. In other states, Br output is inhibited and forced to 1’s (tri-state condition).

**LT Mode Requirement:** During the activation sequence the Rev 3.x device in LT mode sends scrambled “0s” until it reaches states J7 or J8 as required by T1.601. The device then transparently sends Bx data to the line during the late activation stages (J7, J8, J9, J11 only). Similarly the line input data is sent out to Br pin in the same states. In other states, Br output is inhibited and forced to 1’s (tri-state condition).

#### Optional Transparency Control

In certain applications, it may be desirable to have additional control of transparency. This is achieved using the DD bit (Data Disabling) to disable transparency in the CR2 register.

Set DD to 1 (in CR2 register) before activation and set it to 0 after AI interrupt to restore transparency.

Even if 2B + D test mode loopback is requested in the absence of an S interface link, the received act has to be set to 1 (according to the latest proposal in T1.601 spec.).

#### 4.10 2B (128 kbps) and 2B + D (144 kbps) Operation

Contiguous 2B channels (128 kbps) or 2B + D (144 kbps) channel is supported in TP3410 Rev 3.x devices, for all DSI formats 1, 2, 3 and 4, provided the time slots selected can be grouped within time slots 0–3 or 4–63. The time slots 0–3 will have 1 additional 8 kHz frame delay with respect to time slots 4–63.

#### B and D Channel Data Delays Through the Chip

The TP3410 transmitter adds an equal delay for all time slots of 2 to 3 frames (8 kHz) delay. This applies to data sent from the Bx input to the U line output. The receiver, from line input to the Br output, however, has 3 to 4 frames delay for time slots 0–3, and 2 to 3 frames delay for time slots 4–63. This differential delay in receive time slots 0–3 relative to other time slots needs to be considered when designing systems using multiple time slots.

The total delay from the digital interface input (Bx) of one UID chip, to the digital output (Br) of another UID chip at the far end is as follows: 5 frames (625  $\mu$ s) for time slots 0–3 and 6 frames (750  $\mu$ s) for time slots 4–63. The differential delay is also apparent when doing line loopbacks (LB1, LB2 and LBD) for B1, B2 and D. Note for the D channel, the delays are also dependent on time slot position.

The digital loopbacks (DB1, DB2 and DBD) do not show the differential delay between time slots. This loopback is an effective short between the Bx input to the Br output during the chosen time slots.

#### 4.11 Polling the Initial State of RXM4, RXM56 and RXEOC Registers

Normally, change of bit status in any of these registers will cause the appropriate register interrupt and thus provide the updated status of that register. It is not possible to directly readback the values in the RXM4, RXM56 and RXEOC registers.

In LT applications, it is sometimes necessary to know the status of certain bits such as ps1, ps2 bits in the RXM56 registers upon activation to determine the power supply status of the remote NT1 unit. This can be achieved by writing OPR = X’06, causing the RXM56 interrupt on the next superframe boundary to provide the status of the bits in the RXM56 register. After this interrupt the OPR register can be set back to provide an interrupt of RXM56 register only if the status changes and is validated for 3 repetitions (OPR = X’1E).

A similar approach can be used to obtain the status of the RXM4 and RXEOC registers, if required.

#### 4.12 LSD Noise Immunity Considerations

Because of the high sensitivity required by the 10 kHz wake-up tone detector for long loop operation, care needs to be taken to prevent false triggering of this circuit, perhaps due to noise from the line or printed circuit board, or excessive levels of crosstalk.

After initialization, a false LSD at the LT can cause the device to bypass the generation of the TL tone if a local activation is initiated. Similarly, a false LSD condition at the NT can remain latched in the device (unless cleared by an AR command). It is therefore recommended to mask off interrupts from the UID while it is being initialized, and then to reset the LSD circuit by writing X'1E48 or RES command at the end of the initialization sequence.

A spurious LSD triggered condition can be cleared by any of the following sequences:

1. RES, PDN (or PUP)
2. PUP, X'E48, 5 ms delay,
3. PUP, AR
4. PDN (Rev 3.2)

#### 4.13 RES Command Reset Device or to Force A Cold-Start Activation Sequence

The RES command can be used to force the device to reset state after a failed activation attempt or to force a cold-start activation after a successful activation.

1. Resetting the device: The RES command in the Rev 3.x device is operational in the following states for LT mode:- J2, J3, J4, J5, J6; and in NT mode:- H2, H3, H4, H5. The command causes the device to generate an EI interrupt immediately and then jump to J10/H10 state and await loss of signal. After detecting loss of signal (for < 40 ms), there is a state jump to J12/H12 (Receive Reset) which lasts for 40 ms, at the end of which a DI interrupt is generated. So writing a RES command will force the device to stop transmitting and wait for the other end to go silent before generating a local DI Interrupt.
  2. Forcing a cold start and resetting any spurious LSD after deactivation DI.
- Microwire Mode, write: **RES, PDN** (or PUP if staying in PUP state)

— GCI mode: write RES, Delay 5 ms, PDN (or PUP if staying in PUP state)

When used to reset the LSD circuitry, no delay is required between RES and PDN (PUP) for microwire mode.

#### 4.14 DSI Slip Buffer

TP3410 buffers the 2B+D data at the Digital Interface in elastic serial FIFOs, which are 3 frames deep in each direction. When the Digital Interface is a timing slave these FIFOs compensate for relative jitter and wander between the Digital Interface clocks (BCLK and FSA/b) and bit and frame timing at the Line Interface. Each buffer can absorb wander up to 18  $\mu$ s in  $\geq 10$  secs without "slip", exceeding CCITT recommendation Q.502.

Excessive wander causes a controlled slip of one complete frame. It is possible to poll the test register TRG3 to verify if and where a "slip" occurred by writing X'1700. The value of the test register will be returned by servicing the corresponding readback interrupt with value 17xx. The bit7 = 1 of xx indicates RXSLIP and bit6 = 1 of xx indicates TXSLIP has occurred. TXSLIP is in the direction from Bx input to line output, and correspondingly, RXSLIP indicates the direction from line input to Br output.

#### 4.15 Loop Tear-Down and Line Break Conditions

Normal Loop Deactivation or Tear-Down occurs when the LT end equipment initiates an orderly transition to the reset state. The LT end device sends out SL3 frames with "dea" = 0 for at least 3 superframes and then stops transmitting any signal. A TP3410 in LT mode sends 4 superframes with "dea" = 0 before ceasing transmission. The NT end device detects the "dea" = 0 condition, freezes its internal adaptive loop coefficients and prepares for loss-of-signal condition.

In many applications in North America, however, the U interface loop is activated permanently, and a loop deactivation in these applications only occurs if the Loop is broken accidentally (or by deliberately pulling out the cord from the unit). The equipment needs to recover to the reset condition after the line break to support a new activation sequence.

**After a line break, the Rev 3.x device recovers to the reset condition with minimum software intervention as described in Sections 2 and 3 of Part II of this manual.**

#### 4.16 Reading Back TP3410 Activation States

Some applications, such as U-interface Testers, can make use of the ability to determine the activation state of the chip. To read back the state, follow these steps:

a. As part of device initialization (see software reset sequence in Section 1.1) write X'100C or X'100E (if internal 15s timer is also to be disabled).

b. Then write X'1B00 to request read-back of the device status register. Subsequent interrupt servicing will return X'1Bxx where the byte xx is interpreted as shown in the table below:

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	= 1 warm start	SD3	SD2	SD1	SD0

#### State Table Interpretation:

				LT MODE		NT MODE	
SD3	SD2	SD1	SD0	State	Explanation	State	Explanation
0	0	0	0	J1	Reset2	H1	Reset2
0	0	0	1	J41	Wait SN2	H31	Wait SL
0	0	1	0	J42	Check SN2	H32	Check SL
0	0	1	1	J2	Alerting, Send TL	H2	Alerting, Send TN
0	1	1	1	J3	Awake	H3	EC Training
1	1	1	1	J4	EC Training	H4	EC Converged
1	1	1	0	J5	EC Converged	H6	ISW Sync (Tx act = 0) [AP]
1	0	1	0	J6	SW Sync	H5	SW Sync
1	1	0	1	J7	ISW Sync (Rx act = 0, Tx act = 0) [SYNC]	H7	Pending Active (Rx act = 0, Tx act = 1)
1	1	0	0	J8	Active (Tx and Rx act = 1) [AI]	H8	Active (Tx and Rx act = 1) [AI]
0	1	1	0	J9	Deact (Tx dea = 0)	—	—
1	0	0	0	J11	Pending Deact	H9	Pending Deact (Rx dea = 0) [DP]
0	1	0	0	J10	Tear-Down	H10	Tear-Down
1	0	0	1	J12	Rx Reset	H12	Rx Reset
0	1	0	1	—		H11	Error

[xx] denotes status interrupt generated just before device enters this state e.g. [AP], [SYNC].

#### 4.17 Digital System Loopback Conditions

The digital system loopbacks work fine for individual B1, B2 and D channels (controlled by DB1, DB2 and DBD bits in CR3 register) in any format and for any time slot, and with FSa and FSb offset from each other (LT Slave mode).

However, if 2B+D total systems loopback is desired in LT Slave mode (for some applications), it is necessary to have the FSa coincident with FSb, in order to ensure that the B1+B2+D have equal transition delays in their loopback paths through the device.

In normal operation, if the FSa and FSb are not coincident, it may be necessary to switch (by external gating) to coincident FSa and FSb during the 2B+D loopback mode for correct operation. It may also be possible to switch to Line loopbacks at a different point to implement the loopback function.

If all time slots selected are within the group TS0–3 or are all within the group TS4–31, then the FSa/FSb do not need to be coincident for 2B+D loopback.

#### 4.18 RSFS Received Superframe Synch Clock

The RSFS signal indicates the start of each 12 ms receive superframe from the U Interface and is available in NT and LT modes. The Received Superframe Synch clock output is accessible on pin 25 by writing X'1C04 and X'100C (or X'100E) during device initialization. See section 1 for additional device initialization commands. The mode of the transmit superframe synch (TSFS) clock on pin 22 is controlled by SSS bit 7 in the CR2 register.

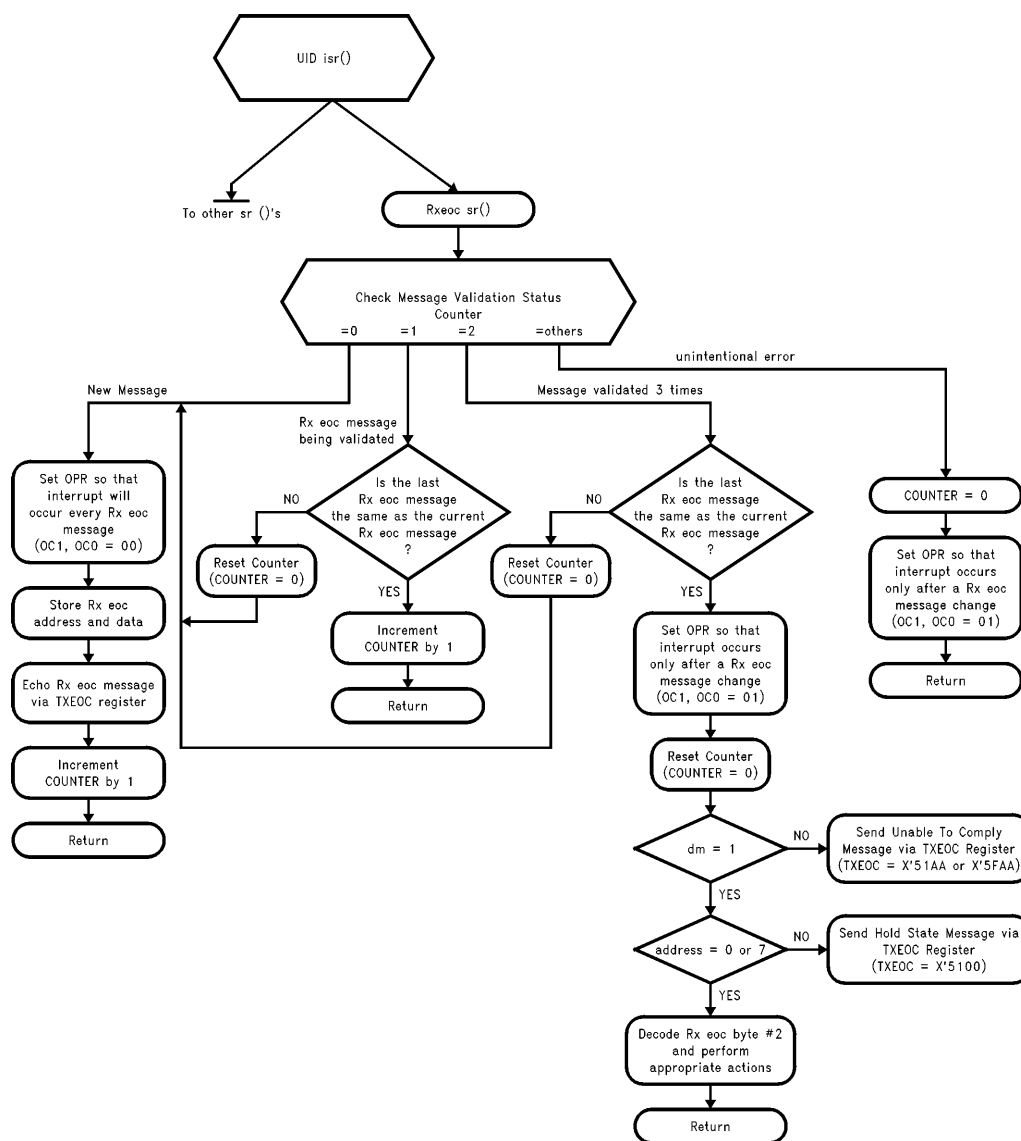
#### 4.19 NT RXEOC Control Flowchart

The ANSI T1.601 standard imposes some time critical conditions to treating received EOC messages at the NT end device. These can be accommodated with a combination of device features and firmware driver routine. The TP3410 provides a number of options in handling validation of EOC messages. The driver flow chart is shown on following page.

In general, the message validation control bits OC1, OC0 in the OPR register have to be alternated between 00 condition (generate RXEOC interrupt every EOC message, 6 ms) to 01 (generate RXEOC interrupt when a change in the received EOC message is detected). A received EOC mes-



# NT Mode EOC Processing Flowchart



TL/H/11933-21

**Note 1:** TXEOC/RXEOC = X'aabb  
aa = Byte 1 contains address, message/data bit  
yy = Byte 2 contains message.

**Note 2:** OC1, OC0 are control bits in OPR Register (see details in TP3410 Data Sheet)

**Note 3:** COUNTER variable indicates message validation status, and must be initialized to X'0 at power-up.

sage has to be acknowledged immediately with an ECHO response via the TXEOC register, followed by proper response to a correctly validated message (i.e., when the same message is received 3 times with a valid address of 0 or 7).

#### 4.20 Interworking and Data Transparency

All TP3410 Rev 3.x devices (Rev 3.2, 3.3 and 3.4) transparently pass data both from the Bx input pin to the U interface and from the U interface to the Br output pin **in full compliance with the ANSI T1.601 standard**. The Rev 3.2 and Rev 3.3 devices also **validate the reception of the correct B-channel data pattern** during start-up. These data patterns are specified for both NT and LT in ANSI T1.601 and are used to help confirm successful completion of the start-up training sequence. In LT mode, the device checks for the reception of "1"s before it can transition to the J6 state and complete synchronization, and similarly in NT mode, the device validates "0"s before transitioning to the H6 state.

Rev 3.4 devices **do not validate the data pattern**. Rev 3.4 parts do not require a far-end interworking device to comply with the start-up data polarity standard of ANSI T1.601. **This data validation is the only difference between Rev 3.3 and Rev 3.4 devices.**

Rev 2.8 devices in NT mode became transparent earlier in the training sequence as described in section 3.6 of TP3410 user's manual Rev C. The solution recommended there was to set the DD = 1 bit in CR2 register during the activation and then set it to DD = 0 when data transparency is required usually after full activation AI = 1, or when maintenance loopbacks are required in the H6/J6 or H7/J7 states. For correct interworking between Rev 2.8 and Rev 3.2 or Rev 3.3 devices the above recommendation must be followed for Rev 2.8 devices particularly with Rev 2.8 at the NT end.

When performing a loopback in the absence of an active S Interface link (UID start-up states H6/J6), use the command X'1610 to enable UID transparency for loopbacks in either the UID or the SID. Use X'1600 to remove transparency when the loopback is removed. These commands are appropriate for all Rev 3.x devices.

#### 4.21 NT Software H9 State

The most recently updated ANSI T1601 Appendix state table allows for a return path for transitions from initial states

H6, H7, H8 or H11 to the H9 state (Pending Deactivation) provided the appropriate conditions are met. See the standard for clarifications. This feature is a minor enhancement to the standard to prevent a "hang-up" in state H9 which may occur if no signal loss can be detected while in this state. The TP3410 Revs 3.3 and 3.4 have a control bit to allow the NT unit to maintain the H9 state in software.

In NT mode, while SH9=0 in the CR4 register (default state), a Rev 3.x device in state H6, H7, H8 or H11 enters the H9 state in response to receiving "dea=0" for 3 consecutive superframes and then exits after 60 ms to H12 (to eliminate the possibility of a "hang up condition"). With SH9=1, a TP3410 Rev 3.3 or 3.4 device in state H6, H7, H8 or H11 generates a DP interrupt after receiving the "dea=0" bit but is prevented from transitioning to device state H9. The device deactivates normally in response to loss of signal.

Deactivating in this manner will however cause an NT mode device to perform only a Cold Start on subsequent activation attempts. The WS bit in CR4 may be set=1 to force the device to **attempt** a Warm Start. This function should only be necessary where warm start is preferred but SH9=1 is required.

#### 4.22 LT-Mode Far-End Initiated Start-Up

In LT mode, the response of the driver software to an AP interrupt (detection of the 10 kHz tone indicating a remote start-up attempt), is to write the PUP and AR commands to proceed with the start-up. In Rev 3.x devices it is important to respond to the AP interrupt indication within 5 ms. The PUP and AR sequence must be sent while the 10 kHz tone is present to startup correctly. This is easily achieved in systems where there is one  $\mu$ P to handle a single TP3410.

In a line-card type of product, where multiple UIDs in LT mode share a common  $\mu$ P, each UID is subject to this same 5 ms time constraint. In this type of case it may be difficult to maintain the 5 ms response window. The "AACT" bit in CR4 register is provided to allow the device to self power-up and begin start-up without the need for the software PUP and AR command sequence. This eliminates the need for the 5 ms response window. For consistency of software routines, the software PUP and AR sequence can be used in conjunction with the "AACT" bit in CR4.

#### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
2900 Semiconductor Drive  
P.O. Box 58090  
Santa Clara, CA 95052-8090  
Tel: (800) 272-9959  
TWX: (910) 339-9240

**National Semiconductor GmbH**  
Livvy-Gargan-Str. 10  
D-82256 Fürstentfeldbruck  
Germany  
Tel: (81-41) 35-0  
Telex: 527849  
Fax: (81-41) 35-1

**National Semiconductor Japan Ltd.**  
Sumitomo Chemical  
Engineering Center  
Bldg. 7F  
1-7-1, Nakase, Mihama-Ku  
Chiba-City,  
Ciba Prefecture 261  
Tel: (043) 299-2300  
Fax: (043) 299-2500

**National Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semicondutores Do Brazil Ltda.**  
Rue Deputado Lacorda Franco  
120-3A  
Sao Paulo-SP  
Brazil 05418-000  
Tel: (55-11) 212-5066  
Telex: 391-1131931 NSBR BR  
Fax: (55-11) 212-1181

**National Semiconductor (Australia) Pty. Ltd.**  
Building 16  
Business Park Drive  
Monash Business Park  
Nottingham, Melbourne  
Victoria 3168 Australia  
Tel: (3) 558-9999  
Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.